CM-T3730 CoM

Reference Guide

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Table 1 Revision Notes

Date	Description
May 2011	First release
August 2012	• Integrated CM-T3730 board rev 1.2 changes. • Chapter 2.1 revised: WLAN now supports 802.11n. • Chapter 2.1 revised: Bluetooth standard v4.0 is now supported. • Chapter 2.1 revised: Optional onboard NAND Flash storage device support added. • Figure 1 revised: Block diagram now corresponds with CM-T3730 board rev1.2. • Table 3 revised: Added support for onboard bootable NAND flash based storage. Revised options column. • Table 4 revised: WiFi & Bluetooth Interface section. USB options • A note on valid configuration added to chapter 2.3. • Chapter 3.3.2 renamed and revised: Added support for onboard bootable NAND flash based storage • Table 6 revised: GPMC_WAIT3 signal description revised • Chapter 4.5 and all related tables revised: Description conforms with WIFI+BT solution used with CM-T3730 board rev1.2. • Table 7 revised: Display interface signals availability changed. • Table 18 revised: UART2 & UART1 signals availability changed. • Table 21 revised: MMC-2 & MMC-3 signals availability changed. • Table 24 revised: GPIO 140, 141, 142, 143, 70, 71, 72, 73 signals availability changed. • Table 28 revised: McBSP3 signals availability changed. • Table 42 minor mistakes fixed: Pin# 68 LCD function is D1 and not D0. • Chapter 4.10 revised. MMC-1 information added. • Table 41 revised: Pins # P1-12, P1-13, P1-15, P1-16, P1-18 P2-4 information added. • Table 42 revised: Pin # P1-10, P1-12, P1-13, P1-15, P1-16, P1-18 information added. • Table 43 revised: Pin # P2-4 information added. • Chapter 4.13: changed number of available GPIOs to 104. • Chapter 4.13: Added note on GPIO120..125 signals. • Chapter 4.10: Added note on MMC1 signals. • Figure 4 updated to correspond with CM-T3730 board revision 1.2 • Figure 5 updated to correspond with CM-T3730 board revision 1.2

Please check for a newer revision of this manual at CompuLab's web site – http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab's CM-T3730 Computer-on-Module.

1.2 CM-T3730 Part Number Legend

Please refer to the CompuLab website 'Ordering Information' section to decode the CM-T3730 part number: http://compulab.co.il/products/computer-on-modules/cm-t3730/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CM-T3730 Product Developer Resources	http://www.compulab.co.il/
AM/DM37x Technical Reference Manual	http://www.ti.com/
TPS65930 Technical Reference Manual	http://www.ti.com/

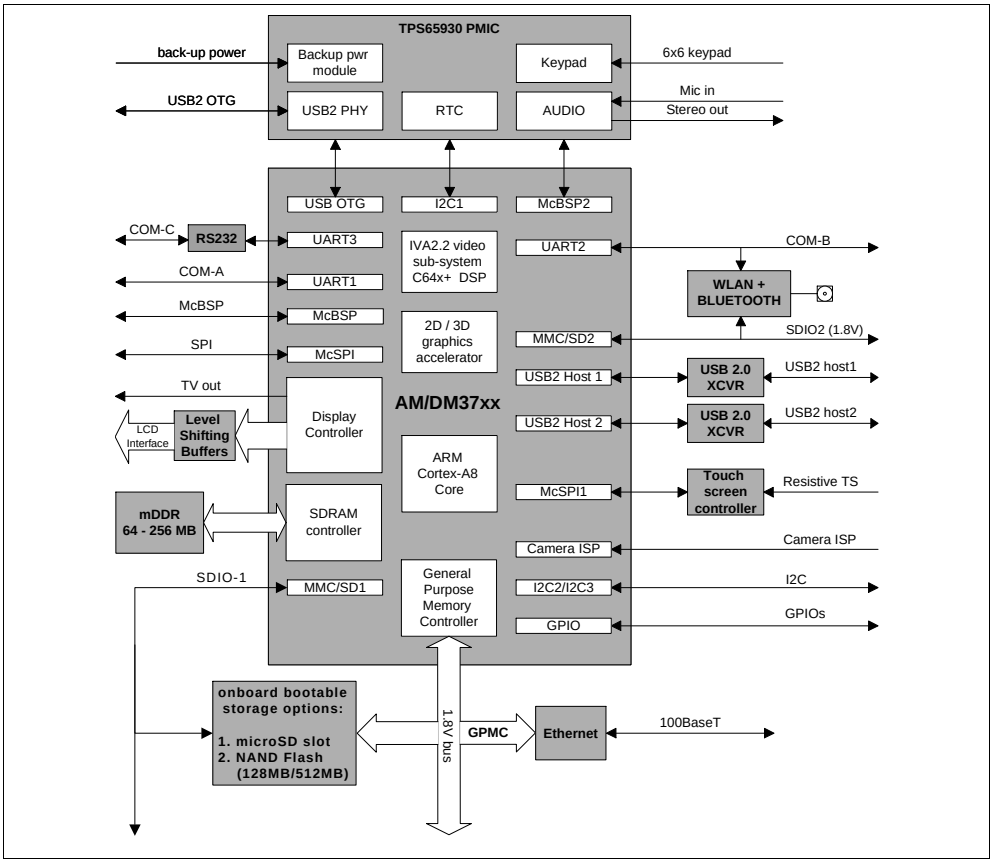
2 OVERVIEW

2.1 Highlights

• Cortex-A8 DM3730 or AM3703 CPU, up to 1000 MHz • Up to 256 MB mobile DDR • Flexible onboard storage options: Up to 512MB SLC NAND Flash or a micro-SD socket onboard. • WLAN / WiFi 802.11b/g/n Interface • Bluetooth 4.0 interface • Graphics controller supporting STN and TFT panels with 1400 x 1050 max resolution • H.264, H.263, MPEG-4, MPEG-2, JPEG, WMV9 and additional video codecs implemented by IVA2.2 Subsystem using TMS320C64x+ DSP core @ 800 MHz • PowerVR SGX GPU providing 2D / 3D graphics acceleration with OpenGL-ES and OpenVG support • General purpose bus • SDIO / MMC interface • Camera Interface port • Sound codec with speaker and microphone support • Touchscreen Controller • USB OTG and Host ports • Serial ports, GPIO • 100 Mbps Ethernet port • Very low standby and active power consumption • Tiny size: 66 x 44 x 7 mm • Interchangeable with other modules via CAMI connectors • SB-T35 Baseboard turns the CM-T3730 module into ***SBC-T3730*** - a tiny single board computer	CM-T3730 is a small Computer-on-Module board designed to serve as a building block in embedded applications. The CM-T3730 is equipped with all the components required to run operating systems such as Linux and Windows CE. Ready packages for these operating systems are available from CompuLab. The small size and low power consumption of CM-T3730 allow its integration into hand-held and mobile devices, while its low price, high MTBF and rich IO make it an ideal selection for cost-sensitive embedded applications. With NAND flash or micro-SD based storage , CM-T3730 provides flexible on-board storage solution and high accessibility for SW filed updates. CM-T3730 is based on TI's 1GHz DaVinci DM3730 / 800MHz Sitara AM3703 processor which combines up to two CPU cores in single package - an advanced Cortex-A8 ARM CPU and TMS32064x DSP for dedicated video processing. TI's new 45nm processors combined with low voltage Mobile DDR enable very low power consumption in regular operation and in standby. CM-T3730 I/O provides a general purpose local bus, 100Mbit Ethernet, serial ports, GPIOs and other essential functions, while integrated WiFi & Bluetooth interfaces implement industry standard wireless connectivity. The standardized CAMI ("CompuLab's Aggregated Module Interface") connectors of the CM-T3730 module allow interchangeability with other Computer-On-Module's available from CompuLab, enabling the flexibility required in a dynamic market where application requirements can change rapidly.

2.2 Block Diagram

Figure 1 CM-T3730 Block Diagram



2.3 CM-T3730 Features

The "Option" column specifies the configuration code required to have the particular feature. "+" means that the feature is always available.

Table 3 CPU, Memory and Busses

Feature	Specifications	Option
CPU	Texas Instruments AM3703 (800MHz) or DM3730 (1GHz with DSP and PowerVR SGX) CPU NEON™ SIMD Coprocessor L1 cache: 112 KB (DSP), 64 KB (ARM) L2 cache: 96 KB (DSP), 256 KB (ARM) DMA, Interrupt controllers, Timers	C1000M C800
RAM	64 - 256 MB, Mobile DDR, 166 MHz, 32-bit	D64 D128 D256
Onboard Storage	An onboard µ-SD socket	NS0G
	An onboard µ-SD socket incl. an 8GB pre-flashed µ-SD card	NS8G
	Onboard 128MBytes bootable SLC NAND Flash	N128
	Onboard 512MBytes bootable SLC NAND Flash	N512
External local bus	16-bit, variable rate up to 133 MHz, 1.8V levels	+

Table 4 Peripherals

Feature	Specifications	Option
Graphics Controller	4/8/16/24 bit color, resolution up to 1400 x 1050, frame buffer in system DDR. Display types support : TFT (parallel RGB), STN, composite video - PAL / NTSC	+
Video acceleration	IVA2.2 Subsystem TMS320C64x+ DSP core running at rate up to 800 MHz. Supporting H.264, H.263, MPEG-4, MPEG-2, JPEG, WMV9 and additional codecs. Part of DM3730 CPU	C1000M
2D / 3D graphics acceleration	PowerVR SGX GPU providing 2D / 3D graphics acceleration with OpenGL-ES and OpenVG support. Part of DM3730 CPU	C1000M
Camera Interface	Direct camera sensor support, max resolution 4096 x 4096, pixel clock up to 130MHz. BT.601 / BT.656 Digital YCbCr 4:2:2 (8/16-Bit) interface.	+
USB	- Host / Slave (OTG) USB2 high-speed port, 480 Mbps	+
	- Additional two USB2 host ports, 480 Mbps, EHCI compliant	U
Serial Ports (UARTs)	3 UART ports, 16550 compatible: COM-A – 1.8V interface, partial modem controls, 3.6 Mbps COM-B – 1.8V interface, partial modem controls, 3.6 Mbps COM-C – 1.8V / RS232 interface, Rx / Tx only, 250 Kbps	+
General Purpose I/O	Up to 98 lines shared with other functions. Can also be used as interrupt inputs	+
Keyboard & mouse	USB, keypad or redirection from COM port	+
Ethernet	SMSC LAN9220 MAC & PHY, 10/100BaseT, Activity LED's	E
MMC / SD	MMC / SD / SDIO support including SDHC up to 32GB, **in addition to the onboard storage**	~~W~~
Audio codec	I2S compliant audio codec, stereo output, differential mic input	+
Touchscreen ctrl.	TSC2046 touchscreen controller. Support 4-wire resistive panels	I
RTC	Real Time Clock, powered by external lithium battery	+
WiFi & Bluetooth Interface	Implements 802.11b/g/n wireless connectivity standard. Ad-Hoc and Infrastructure modes. Based on TI WiLink6.0 WL1271 solution. On-board connector for external antenna. Bluetooth 4.0 (also compliant with Bluetooth 2.1 + EDR)	W

NOTE: A valid configuration must contain one CPU option, one RAM option and one Onboard Storage option.

Table 5 Electrical, Mechanical and Environmental Specifications

Supply Voltage	Single 3.8V or Lithium-ion polymer battery
Active power consumption	0.2 - 2 W, depending on configuration and CPU speed
Standby/Sleep consumption	20 - 100 mW, depending on configuration and mode
Dimensions	66 x 44 x 7 mm
Weight	16 gram
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0^{o} to 70^{o} C Extended: -20^{o} to 70^{o} C Industrial: -40^{o} to 85^{o} C
Storage temperature	-40^{o} to 85^{o} C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	2 x 140 pin, 0.6 mm
Connector insertion / removal	50 cycles

NOTE: Ordering an Extended/Industrial temperature version of CM-T3730 precludes the NS8G (8GB micro-SD) option. For detailed instructions on bootable micro-SD preparation, please refer to CompuLab website.

3 CORE SYSTEM COMPONENTS

3.1 AM37xx / DM37xx CPU

The TI DM37xx / AM37xx generation of high-performance, applications processors are based on the enhanced device architecture and are integrated on TI's advanced 45-nm process technology.

The architecture is designed to provide video, image, and graphics processing sufficient to support the following:

- Streaming video
- 2D/3D mobile gaming
- Video conferencing
- High-resolution still images
- Video capture in wireless terminals, multimedia-featured handsets, and high-performance personal digital assistants (PDA's).

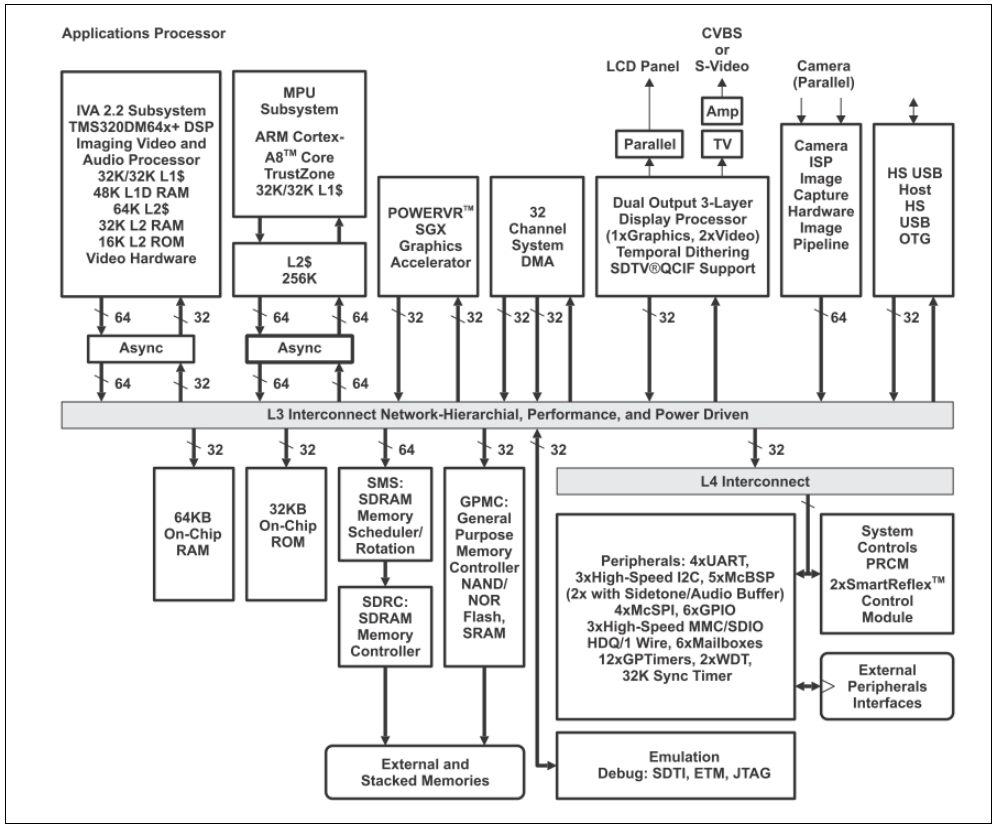
This device includes power-management techniques required for high-performance mobile products.

The following subsystems are parts of the device:

- Microprocessor unit (MPU) subsystem based on the ARM® Cortex™-A8 microprocessor
- IVA2.2 subsystem with a C64x+ digital signal processor (DSP) core (DM37xx only)
- SGX subsystem for 2D and 3D graphics acceleration to support display and gaming effects (DM37xx only)
- Camera image signal processor (ISP) supporting multiple formats and interfacing options to a wide variety of image sensors
- Display subsystem with multiple concurrent image manipulation support, and a programmable interface supporting a wide variety of displays. The display subsystem also supports NTSC/PAL video out.
- Level 3 (L3) and level 4 (L4) interconnects that provide high-bandwidth data transfers for multiple initiators to the internal and external memory controllers and to on-chip peripherals

The device also offers a comprehensive power and clock-management scheme that enables high-performance, low-power operation and ultralow-power standby features. The device also supports SmartReflex™ adaptive voltage control.

Figure 2 DM37xx Block Diagram



3.2 Multimedia System

3.2.1 IVA2.2 Subsystem

The DM3730 includes a high-performance imaging video and audio (IVA2.2) accelerator based on the Texas Instruments TMS320DMC64x+ VLIW DSP core.

For additional details, please refer to section 5 of the "AM/DM37x Technical Reference Manual".

3.2.2 Multimedia Accelerator

The DM3730 2D and 3D graphics accelerator (SGX) provides support for the following imaging and video features:

- 2D and 3D graphics and video codecs supported on common hardware
- Tile-based architecture
- An advanced shader feature set in excess of Microsoft VS3.0, PS3.0 and OGL2.0
- Industry standard API supports Direct3D mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0 and OpenMax
- Fine-grained task switching, load balancing and power management
- Programmable high-quality image anti-aliasing
- Advanced geometry DMA driven operation for minimum CPU interaction
- Fully virtualized memory addressing for OS operation in a unified memory architecture
- Advanced and standard 2D operations (that is, vector graphics, BLT's, ROP's, etc.)
- Programmable video encode and decode support for H.264, H.263, MPEG4 (SP), WMV9 and JPEG

NOTE: Multimedia features are available only with the 'C1000M' configuration option.

3.3 Memory

3.3.1 DRAM

CM-T3730 is available with 64, 128 or 256 Mbytes of mobile DDR. The DDR interface is 32-bits wide and runs with a 166 MHz clock.

3.3.2 Onboard Storage.

CM-T3730 is equipped with one of the following onboard storage solutions:

- 128 or 512 Mbytes of SLC NAND Flash with boot-loader software.
- Onboard micro-SD socket. An 8GB micro-SD card, pre-flashed with boot-loader software can optionally be included with this option.

The onboard storage solution of choice, serves as the main non-volatile memory device of CM-T3730. This non-volatile storage is used for storing the boot-loader and the OS.

NOTE: Ordering an Extended/Industrial temperature version of CM-T3730 precludes the NS8G (8GB micro-SD) option. For detailed instructions on bootable micro-SD preparation, please refer to CompuLab website.

3.4 PMIC

The CM-T3730 features the TI TPS65930 companion chip for AM/DM37xx power management and additional peripheral devices.

The TPS65930 is a power-management IC for AM/DM73xx™ and other mobile applications. The device includes power-management, a high-speed USB transceiver, LED drivers, an ADC, a real-time clock and embedded power control (EPC) and a keypad controller. In addition, the TPS65930 includes a full audio codec with two DAC's and two ADC's to implement dual voice channels, and a stereo downlink channel that can play all standard audio sample rates through a multiple format inter-integrated sound (I2S™) TDM interface.

The TPS65930 supports the power and peripheral requirements of the AM/DM37xx processor. The power portion of the device contains three buck converters, two of which are controllable by a dedicated SmartReflex™ class-3 interface, multiple LDO regulators, an EPC to manage the power sequencing requirements of AM/DM37xx, an RTC and a backup module. The RTC can be powered by a backup battery when the main supply is not present, and the device includes a coin-cell charger to recharge the backup battery as needed.

4 PERIPHERAL INTERFACES

CM-T3730 implements a number of peripheral interfaces through the baseboard interface connectors (P1 and P2). The following notes apply to those interfaces:

- Some interfaces/signals are available only with/without certain configuration options of the CM-T3730. Each signal's availability is noted in the "Signals description" table of each interface.
- Most baseboard interface pins can be configured as one of several signals. For pin multiplexing characteristics, please refer to chapter 5.7.
- Certain signals are available on more than one baseboard interface pin. Only one pin can be used for each signal.
- All of the CM-T3730 digital interfaces operate at 1.8V voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" tables. The following notes summarize the column headers for these tables:

- **"Signal name"** – The symbolic name of each signal
- **"Pin#" –** The pin number on the baseboard interface connectors
- **"Type" –** Signal type
- **"Description" –** Signal description
- **"Availability" –** Certain signals are not available with/without certain configuration options. This column summarizes configuration requirements for each signal.

Each baseboard interface signal can be one of the following types. Signal type is noted in the "Signal description" tables for each signal

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"OD"** – Open Drain Signal (not pulled up onboard CM-T3730 unless otherwise noted).
- **"P"** – Power
- **"PU18"** – Always pulled up to 1.8V onboard CM-T3730
- **"PU33**" – Always pulled up to 3.3V onboard CM-T3730
- **"PUMMC"** – Always pulled up to VCC_MMC onboard CM-T3730
- **"PD" -** Always pulled down onboard CM-T3730

4.1 Local Bus

The CM-T3730 local bus is derived from the AM/DM37xx general-purpose memory controller (GPMC) bus. GPMC is dedicated to interfacing with the following external memory devices:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous, synchronous and page mode (only available in non-muxed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For additional details, please refer to section 10.1 of the "AM/DM37x Technical Reference Manual".

Table 6 Local bus signals

Signal Name	Pin #	Type	Description	Availability
GPMC_A1	P1-71*	O	Address bit 1	Always available
GPMC_A2	P1-70*	O	Address bit 2	Always available
GPMC_A3	P1-73*	O	Address bit 3	Always available
GPMC_A4	P1-72*	O	Address bit 4	Always available
GPMC_A5	P1-75*	O	Address bit 5	Always available
GPMC_A6	P1-76*	O	Address bit 6	Always available
GPMC_A7	P1-77*	O	Address bit 7	Always available
GPMC_A8	P1-78*	O	Address bit 8	Always available
GPMC_A9	P1-81*	O	Address bit 9	Always available
GPMC_A10	P1-80*	O	Address bit 10	Always available
GPMC_D0	P1-94	IO	Data bit 0	Always available
GPMC_D1	P1-95	IO	Data bit 1	Always available
GPMC_D2	P1-96	IO	Data bit 2	Always available
GPMC_D3	P1-97	IO	Data bit 3	Always available
GPMC_D4	P1-100	IO	Data bit 4	Always available
GPMC_D5	P1-99	IO	Data bit 5	Always available
GPMC_D6	P1-102	IO	Data bit 6	Always available
GPMC_D7	P1-101	IO	Data bit 7	Always available
GPMC_D8	P1-104*	IO	Data bit 8	Always available
GPMC_D9	P1-105*	IO	Data bit 9	Always available
GPMC_D10	P1-106*	IO	Data bit 10	Always available
GPMC_D11	P1-107*	IO	Data bit 11	Always available
GPMC_D12	P1-108*	IO	Data bit 12	Always available
GPMC_D13	P1-109*	IO	Data bit 13	Always available
GPMC_D14	P1-112*	IO	Data bit 14	Always available
GPMC_D15	P1-111*	IO	Data bit 15	Always available
GPMC_nCS3	P1-92*	O	Chip select bit 3	Always available
GPMC_nCS4	P1-93*	O	Chip select bit 4	Always available
GPMC_nCS7	P1-85*	O	Chip select bit 7	Always available
GPMC_IODIR			IO direction control for use with external transceivers	
GPMC_CLK	P1-88*	O	Clock	Always available
GPMC_nADV	P1-90	O	Address valid	Always available
GPMC_ALE			Address latch enable for NAND protocol memories	
GPMC_nOE	P1-89	O	Output enable	Always available
GPMC_nWE	P1-84	O	Write enable	Always available
GPMC_nBE0	P1-82*	O	Lower byte enable	Always available
GPMC_nCLE			Command latch enable for NAND protocol memories	
GPMC_nBE1	P1-87*	O	Upper byte enable	Always available
GPMC_WAIT3	P1-83*	I	External wait signal for NOR and NAND protocol memories	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.2 Display Interface

The CM-T3730 display subsystem is based on the display interface of the AM/DM37xx.

The display subsystem provides the logic to display a video frame from the memory frame buffer (either SDRAM or SRAM) on either a liquid-crystal display (LCD) panel or a TV set.

The display subsystem supports the following main features:

Display controller

- Programmable pixel display modes (1, 2, 4, 8, 12, 16 and 24 bits-per-pixel)
- Programmable panel size up to 2048 (lines) x 2048 (pixels)
- 256 x 24-bit entries palette in red, green and blue (RGB)
- Programmable pixel rate up to 75 MHz
- Four types of displays are supported: passive (STN) and active (TFT) colors, passive (STN) and active (TFT) monochromes
- Overlay support for graphics
- Programmable video re-sizer independent horizontal and vertical re-sampling
- Rotation of 90-, 180- and 270-degrees

Video encoder

- NTSC/PAL encoder outputs with the following standards:
  - NTSC-J, M
  - PAL-B, D, G, H, I
  - PAL-M
  - CGMS-A as described in the CEA-608-x standard
- Composite video (CVBS)
- Separate video (S-video)

For additional details, please refer to section 7 of the "AM/DM37x Technical Reference Manual".

The LCD_VIO pin supplies power to the LCD interface, allowing configuration of the operating voltage levels for LCD interface signals. The operating voltage can be set to 1.8V, 2.5V or 3.3V.

NOTE: LCD interface logic levels are set according to the LCD_VIO pin input voltage.

Table 7 Display interface signals

Signal Name	Pin #	Type	Description	Availability
LCD interface				
LCD_PCLK	P2-112	O	Pixel clock	Always available
LCD_HSYNC	P2-96	O	Horizontal synchronization	Always available
LCD_VSYNC	P2-111	O	Vertical synchronization	Always available
LCD_ACBIAS	P2-114	O	AC bias control (STN) or pixel data enable (TFT)	Always available
LCD_D0	P2-95	O	Pixel data bit 0	Always available
	P1-58*	IO		Only available **without 'W'** option
LCD_D1	P2-97	O	Pixel data bit 1	Always available
	P1-68*	IO		Only available **without 'W'** option
LCD_D2	P2-100	O	Pixel data bit 2	Always available
	P1-113*	IO		Only available **without 'W'** option
LCD_D3	P2-99	O	Pixel data bit 3	Always available
	P1-118*	IO		Only available **without 'W'** option
LCD_D4	P2-102	O	Pixel data bit 4	Always available
	P1-129*	IO		
LCD_D5	P2-101	O	Pixel data bit 5	Always available
	P2-64*	IO		
LCD_D6	P2-104	O	Pixel data bit 6	Always available
LCD_D7	P2-106	O	Pixel data bit 7	Always available
LCD_D8	P2-105	O	Pixel data bit 8	Always available
LCD_D9	P2-108	O	Pixel data bit 9	Always available
LCD_D10	P2-107	O	Pixel data bit 10	Always available
LCD_D11	P2-109	O	Pixel data bit 11	Always available
LCD_D12	P2-113	O	Pixel data bit 12	Always available
LCD_D13	P2-116	O	Pixel data bit 13	Always available
LCD_D14	P2-118	O	Pixel data bit 14	Always available
LCD_D15	P2-117	O	Pixel data bit 15	Always available
LCD_D16	P2-120	O	Pixel data bit 16	Always available
LCD_D17	P2-119	O	Pixel data bit 17	Always available
LCD_D18	P2-124	O	Pixel data bit 18	Always available
LCD_D19	P2-121	O	Pixel data bit 19	Always available
LCD_D20	P2-126	O	Pixel data bit 20	Always available
LCD_D21	P2-123	O	Pixel data bit 21	Always available
LCD_D22	P2-94	O	Pixel data bit 22	Always available
LCD_D23	P2-93	O	Pixel data bit 23	Always available
LCD_VIO	P2-16	P	Power supply input for LCD interface. Connect to 1.8V / 2.5V / 3.3V power rail. The power source must provide 150mA continuous current.	Always available
Video encoder				
TV_OUT1	P2-1	AO	TV analog output composite	Always available
TV_OUT1	P2-3	AO	TV analog output S-VIDEO	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

NOTE: Pins denoted with "*" cannot be used as display interface signals under certain conditions. For details, please refer to section 7 of "AM/DM37x Technical Reference Manual"

NOTE: Pins denoted with "*" reference voltage is independent of LCD_VIO pin setting. The signal at these pins is always 1.8V referenced.

4.3 Ethernet

The CM-T3730 incorporates a single full-featured 10/100 Ethernet interface, implemented with the SMSC LAN9220 Ethernet controller.

The CM-T3730 Ethernet interface supports the following main features:

- Fully compliant with IEEE 802.3/802.3u standards
- 10BASE-T and 100BASE-TX
- Full- and Half-duplex
- HP Auto-MDIX
- Activity and speed indicator LED controls

Table 8 Ethernet interface signals

Signal Name	Pin #	Type	Description	Availability
CM_ETH_TXP	P1-1	AO, PU33	Transmit positive output	Only available **with** 'E' option.
CM_ETH_TXN	P1-3	AO, PU33	Transmit negative output	Only available **with** 'E' option.
CM_ETH_RXP	P1-4	AI, PU33	Receive positive input	Only available **with** 'E' option.
CM_ETH_RXN	P1-2	AI, PU33	Receive negative input	Only available **with** 'E' option.
CM_ETH_LED1	P1-6	OD	Activity indicator LED output. Active low.	Only available **with** 'E' option.
CM_ETH_LED2	P1-5	OD	Speed indicator LED output. Active (100Mbs) low.	Only available **with** 'E' option.

NOTE: For magnetics' selection recommendations, please refer to section 8.3 of this document.

4.4 USB 2.0

4.4.1 USB 2.0 On-The-Go

The USB 2.0 OTG interface is implemented with the AM/DM37xx USB 2.0 OTG controller. The interface provides the following features:

- Supports USB 2.0 peripheral at High Speed (480 Mbps) and Full Speed (12 Mbps)
- Supports USB 2.0 host at High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps)
- Operates either as the function controller of a high-/full-speed USB peripheral or as the host/peripheral in point-to-point or multipoint communications with other USB functions
- Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the on-the-go (OTG) supplement (Revision 1.0a)

Table 9 USB 2.0 OTG interface signals

Signal Name	Pin #	Type	Description	Availability
USB0_DP	P1-136	AIO	USB OTG positive data	Always available
USB0_DN	P1-138	AIO	USB OTG negative data	Always available
USB0_ID	P1-137	AIO	USB OTG ID	Always available
USB0_5V_OUT	P1-140	P	USB OTG VBUS power rail	Always available

4.4.2 USB 2.0 Host

The CM-T3730 high-speed USB interface is implemented with the AM/DM37xx high-speed USB host subsystem. The interface provides the following features:

- Complies with the USB 2.0 standard for high-speed (480M bit/s) functions
- Complies with EHCI (high-speed host controller)

Up-to two high-speed USB host ports are supported.

NOTE: The USB 2.0 host ports do not support low-speed and full-speed operation modes. External USB hub is recommended in order to enable these operation modes. Please refer to the SB-T35 design package for a comprehensive reference design.

Table 10 USB 2.0 Host interface signals

Signal Name	Pin #	Type	Description	Availability
USB-1				
USB1_DP	P2-138	AIO	USB host port 1 positive data	Only available **with** 'U' option
USB1_DN	P2-140	AIO	USB host port 1 negative data	Only available **with** 'U' option
USB1_CPEN	P2-6	O	USB host port 1 external 5V supply enable. Active high.	Only available **with** 'U' option
USB1_VBUS	P2-8	P	USB host port 1 external 5V supply sense input.	Only available **with** 'U' option
USB-2				
USB2_DP	P2-137	AIO	USB host port 2 positive data	Only available **with** 'U' option
USB2_DN	P2-139	AIO	USB host port 2 negative data	Only available **with** 'U' option
USB2_CPEN	P2-9	O	USB host port 2 external 5V supply enable. Active high.	Only available **with** 'U' option
USB2_VBUS	P2-11	P	USB host port 1 external 5V supply sense input.	Only available **with** 'U' option

4.5 WLAN and Bluetooth

CM-T3730 incorporates full-featured 802.11b/g/n and Bluetooth 4.0 capabilities, implemented with the Murata LBEH59XUHC WLAN + Bluetooth combo controller module. The LBEH59XUHC is based on the Texas Instruments WiLink6.0 WL1271 chipset.

WLAN Standards supported:

- 802.11b data rates of 1, 2, 5.5 and 11 Mbps.
- 802.11g data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps.
- 802.11n-2.4G data rates of 6.5, 13, 19.5, 26, 39, 52, 58.5 and 65Mbps.

Bluetooth standards supported:

- Bluetooth 4.0
- Bluetooth Power Class 1

The LBEH59XUHC SiP is interfaced with the Sitara AM3517/05 SoC using the MMC-2 and UART-2 ports. MMC-2 is used for WLAN data while UART-2 is used for Bluetooth data.

Antenna Connection

The LBEH59XUHC requires a single 2.45GHz antenna. The antenna is connected via the onboard UFL high frequency connector J2. Any type of 2.45GHz antenna can be used. Please refer to section 6.3 for connector location.

Table 11 J2 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

Table 12 Test Conditions (Tables 13, 14, 15 and 16)

Parameter	Value
Temperature	25˚C
VCC_CM	3.6V

Table 13 802.11b (WLAN) RF system specifications

TX Characteristics				
Parameter	Min	Typ	Max	Unit
Power Levels	14	16	18	dBm
Spectrum Mask				
1st side lobes		-40	-30	dBr
2nd side lobes		-55	-50	dBr
Power-on and Power-down ramp		0.1	2	µSec
RF Carrier Suppression	15	37		dB
Modulation Accuracy (EVM)		10	35	%
Spurious Emissions				
30MHz to 1GHz		-80	-36	dBm
1GHz to 12.75GHz		-60	-30	dBm
1.8GHz to 1.9GHz		-80	-47	dBm
5.15GHz to 5.3GHz		-80	-47	dBm
RX Characteristics				
Parameter	Min	Typ	Max	Unit
Minimum Input Level Sensitivity				
11Mbps (FER ≤ 8%)		-87	-76	dBm
Maximum Input Level (FER ≤ 8%)	-10	0		dBm

Table 14 802.11g (WLAN) RF system specifications

TX Characteristics				
Parameter	Min	Typ	Max	Unit
Power Levels	11	13	15	dBm
Spectrum Mask				
at fc +/- 11MHz		-30	-20	dBr
at fc +/- 20MHz		-33	-28	dBr
at fc +/- 30MHz		-45	-40	dBr
Spurious Emissions				
30MHz to 1GHz		-80	-36	dBm
1GHz to 12.75GHz		-65	-30	dBm
1.8GHz to 1.9GHz		-80	-47	dBm
5.15GHz to 5.3GHz		-80	-47	dBm
Constellation Error (EVM)		-30	-25	dB
RX Characteristics				
Parameter	Min	Typ	Max	Unit
Minimum Input Level Sensitivity				
54Mbps (PER ≤ 10%)		-73	-65	dBm
Maximum Input Level (PER ≤ 10%)	-20	-4		dBm

Table 15 802.11n (WLAN) RF system specifications

TX Characteristics				
Parameter	Min	Typ	Max	Unit
Power Levels	10	12	14	dBm
Spectrum Mask				
at fc +/- 11MHz		-30	-20	dBr
at fc +/- 20MHz		-35	-28	dBr
at fc +/- 30MHz		-50	-45	dBr
Spurious Emissions				
30MHz to 1GHz		-80	-36	dBm
1GHz to 12.75GHz		-65	-30	dBm
1.8GHz to 1.9GHz		-80	-47	dBm
5.15GHz to 5.3GHz		-80	-47	dBm
Constellation Error (EVM)		-30	-28	dB
RX Characteristics				
Parameter	Min	Typ	Max	Unit
Minimum Input Level Sensitivity				
54Mbps (PER ≤ 10%)		-67	-64	dBm
Maximum Input Level (PER ≤ 10%)	-20	-5		dBm

Table 16 Bluetooth RF system specifications

TX Characteristics				
Parameter	Min	Typ	Max	Unit
Output Power	4.5	8.0		dBm
Frequency range (Rx/Tx)	2400 – 2483.5			MHz
-20db bandwidth		0.8	1	MHz
Adjacent Channel Power (Up to 3 spurious responses within Bluetooth limits are allowed)				
[M-N] = 2		-45	-20	dBm
[M-N] ≥ 3		-46	-40	dBm
Modulation Characteristics				
Modulation δf1avg	140	158	175	kHz
Modulation δf2max	115	132		kHz
Modulation δf2avg/δf1avg	0.8	0.9		kHz
Carrier Frequency Drift				
1 slot	-25		+25	kHz
3 slot	-40		+40	kHz
5 slot	-40		+40	kHz
Maximum drift rate	-20		+20	kHz/ 50µS

TX Characteristics				
Parameter	Min	Typ	Max	Unit
Out-of Band Spurious Emissions				
30-1000MHz (Operation mode)		-58	36	dBm
1000-12750MHz (Operation mode)		-40	-30	dBm
1800-1900MHz (Operation mode)		-80	-47	dBm
5150-5300MHz (Operation mode)		-80	-47	dBm
EDR Relative Power (π/4-DQPSK and 8DPSK)	-4	-0.2	1	
EDR Carrier Frequency Stability and Modulation Accuracy				
ωi (Pi/4-DQPSK and 8DPSK)	-75	0	75	kHz
ω0 (Pi/4-DQPSK and 8DPSK)	-10	0	10	kHz
ωi+ω0 (Pi/4-DQPSK and 8DPSK)	-75	0	75	kHz
RMS DEVM (Pi/4-DQPSK)		6	20	%
99% DEVM (Pi/4-DQPSK)		10	30	%
Peak DEVM (Pi/4-DQPSK)		14	35	%
RMS DEVM (8DPSK)		6	13	%
99% DEVM (8DPSK)		10	20	%
Peak DEVM (8DPSK)		15	25	%
RX Characteristics				
Parameter	Min	Typ	Max	Unit
Sensitivity (BER < 0.1%)				
2402MHz		-90	-70	dBm
2441MHz		-90	-70	dBm
2480MHz		-90	-70	dBm
C/I Performance (BER < 0.1%) (Up to 5 spurious responses within Bluetooth limits are allowed.)				
co-channel ratio (-60dBm input)		7	11	dB
1MHz ratio (-60dBm input)		-9	0	dB
2MHz ratio (-60dBm input)		-46	-30	dB
3MHz ratio (-67dBm input)		-48	-40	dB
image +/- 1MHz ratio (-67dBm input)		-30	-20	dB
Blocking performance (BER < 0.1%) (Up to 24 spurious responses within Bluetooth limits are allowed.)				
30MHz-2000MHz	-10	-8		dBm
2000MHz-2400MHz	-27	0		dBm
2500MHz-3000MHz	-27	0		dBm
3000MHz-12750MHz	-10	-5		dBm
Intermodulation performance (BER < 0.1%, -64dBm input)	-39	-30		dBm
Maximum Input Level	-20	10		dBm
EDR Sensitivity (at 0.01% BER)				
π/4-DQPSK		-90	-70	dBm
8DPSK		-84	-70	dBm

For additional details, please refer to the Murata LBEH59XUHC datasheet.

NOTE: The WLAN & Bluetooth module is available only with the 'W' configuration option.

4.6 Audio

The CM-T3730 audio subsystem is implemented with the audio codec of the TI TPS65930 companion chip. The audio subsystem supports the following features:

- External class-D amplifier pre-driver stereo output
- Differential microphone input
- Single-ended auxiliary input

Table 17 Audio signals

Signal Name	Pin #	Type	Description	Availability
AUDIO_OUT_R	P2-136	AO	Pre-driver output right for external class-D amplifier	Always available
AUDIO_OUT_L	P2-130	AO	Pre-driver output left for external class-D amplifier	Always available
AUDIO_IN	P2-128	AI	Auxiliary audio input	Always available
MIC_IN_P	P2-131	AI	Differential microphone positive input	Always available
MIC_IN_N	P2-133	AI	Differential microphone negative input	Always available
MIC_BIAS	P2-129	AP	Microphone bias	Always available

4.7 UART's

The CM-T3730 incorporates three general purpose UART's. The following features are supported:

- 16C750 compatibility
- 64-byte FIFO for receiver and 64-byte FIFO for transmitter
- Programmable baud rate of up to 3.6M bit/s
- Configurable data format

For additional details on UART interface of the AM/DM37xx, please refer to section 19 of the "AM/DM37x Technical Reference Manual".

NOTE: Using the UART-3 port precludes the use of the RS-232 and IRDA ports.

Table 18 UART signals

Signal Name	Pin #	Type	Description	Availability
UART-1				
UART1_TX	P1-24*	O	UART1 serial data out	Always available
UART1_RX	P1-22*	I	UART1 serial data in	Always available
UART1_CTS	P1-27*	I	UART1 clear to send	Always available
	P1-58*			Only available **without 'W'** option
UART1_RTS	P1-29*	O	UART1 request to send	Always available
	P1-68*			Only available **without 'W'** option
UART-2				
UART2_TX	P1-32*	O	UART2 serial data out	Only available **without 'W'** option
UART2_RX	P1-34*	I	UART2 serial data in	Only available **without 'W'** option
UART2_CTS	P1-33*	I	UART2 clear to send	Only available **without 'W'** option
UART2_RTS	P1-35*	O	UART2 request to send	Only available **without 'W'** option
UART-3**				
UART3_TX	P2-64*	O	UART3 serial data out	Always available
UART3_RX	P1-129*	I	UART3 serial data in	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.8 RS232

The CM-T3730 incorporates a single RS232 port. The following features are supported:

- 16C750 compatibility
- 64-byte FIFO for receiver and 64-byte FIFO for transmitter
- Programmable baud rate of up to 250 kbit/s
- Configurable data format
- RS-232 bus-pin ESD protection exceeds ±15 kV using the Human-Body Model

The RS232 port is derived from UART3 of the AM/DM37xx SoC.

NOTE: The RS232 port operates at RS232 voltage levels.

NOTE: Using the RS-232 port precludes the use of UART-3 and IRDA ports.

Table 19 RS232 signals

Signal Name	Pin #	Type	Description
RS232_TXD	P1-30	O	RS232 serial data out
RS232_RXD	P1-28	I	RS232 serial data in

4.9 IRDA

The CM-T3730 integrated IRDA port is based on the AM/DM37xx port IRDA communication support. CM-T3730 IRDA port supports the following key features:

- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications
- Uplink/downlink cyclic redundancy check (CRC) generation/detection
- Framing error, CRC error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection

For additional details on IRDA interface of the AM/DM37xx, please refer to section 19 of the "AM/DM37x Technical Reference Manual".

NOTE: Using the IRDA port precludes the use of the RS-232 and UART3 ports.

Table 20 IRDA signals

Signal Name	Pin #	Type	Description	Availability
UART3_IRRX	P1-129*	I	Serial data input	Always available
UART3_IRTX	P2-64*	O	Serial data output in SIR, MIR, and FIR modes	Always available
UART3_RTS_SD	P1-42*	O	SD mode is used to configure the transceivers.	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.10 MMC / SD / SDIO

The CM-T3730 features up to three multimedia card high-speed/secure data/secure digital I/O (MMC / SD / SDIO) host interfaces. The following main features are supported:

- Full compliance with MMC command/response sets as defined in the Multimedia Card System Specification, v4.2. including high-capacity (size >2GB) cards HC MMC.
- Full compliance with SD command/response sets as defined in the SD Memory Card Specifications, v2.0. including high-capacity cards SDHC up to 32 GB.
- Full compliance with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10
- Compliance with sets as defined in the SD Card Specification, Part A2, SD Host Controller Standard Specification, v1.00
- Full compliance with MMC bus testing procedure as defined in the Multimedia Card System Specification, v4.2
- Full compliance with CE-ATA command/response sets as defined in the CE-ATA Standard Specification

The MMC/SD/SDIO host controller can support one slave device (MMC memory card, SD memory card or SDIO device).

The first controller (MMC-1) integrates an internal transceiver that allows a direct connection to the MMC/SD/SDIO card (1.8V and 3V) without an external transceiver. The software-controlled VCC_MMC power output pin allows setting the proper operating voltage. The MMC1 interface supports 1 or 4 bit transfer modes for MMC/SD/SDIO cards.

Whenever CM-T3730 configuration includes the ‘NS0G’ or the ‘NS8G’ options, MMC-1 signals are not available at the baseboard interface connectors since they are used for CM-T3730 onboard micro-SD based storage.

The MMC-2 controller interface is used for CM-T3730 WLAN and Bluetooth functionality ("W" product option). MMC-2 allows connecting MMC/SD/SDIO (1.8V logic levels) cards or an external device that uses the MMC/SD/SDIO interface (a WLAN device for example). MMC-2 also supports an external transceiver and provides direction signals for data and command. Using an external transceiver device precludes 8-bit transfer mode.

The MMC-3 controller interface allows connecting MMC/SD/SDIO (1.8V logic levels) cards or an external device that uses the MMC/SD/SDIO interface. MMC-3 does not support 8-bit transfer mode and external transceiver

For additional details, please refer to section 24 of the “AM/DM37x Technical Reference Manual”.

Table 21 MMC / SD / SDIO signals

Signal Name	Pin #	Type	Description	Availability
MMC-1				
MMC1_CLK	P1-12*	O PUMMC	Output clock	• Only available **without** ‘NS8G’ & ‘NS0G’ options • These pins MUST be left floating when CM-T3730 is configured for NS8G or NS0G options. • These pins are not available with CM-T3730 board revisions < 1.2
MMC1_CMD	P1-13*	IO PUMMC	Command signal	
MMC1_DAT0	P1-15*	IO PUMMC	Card data bit 0	
MMC1_DAT1	P1-16*	IO PUMMC	Card data bit 1	
MMC1_DAT2	P2-4*	IO PUMMC	Card data bit 2	
MMC1_DAT3	P1-18*	IO PUMMC	Card data bit 3	
VCC_MMC	P1-10	P	MMC1 dedicated output voltage (1.8V/3V) enabled/disabled by software	

MMC-2				
MMC2_CLK	P1-48*	IO	MMC2 Interface clock	Only available **without** 'W' option
MMC2_CMD	P1-41*	O	Command signal	Only available **without** 'W' option
MMC2_DAT0	P1-46*	IO	Card data bit 0	Only available **without** 'W' option
MMC2_DAT1	P1-47*	IO	Card data bit 1	Only available **without** 'W' option
MMC2_DAT2	P1-52*	IO	Card data bit 2	Only available **without** 'W' option
MMC2_DAT3	P1-49*	IO	Card data bit 3	Only available **without** 'W' option
MMC2_DAT4	P1-54*	IO	Card data bit 4	Only available **without** 'W' option
MMC2_DIR_DAT0		O	Direction signal for DAT0 for use with external transceivers	Only available **without** 'W' option
MMC2_DAT5	P1-39*	IO	Card data bit 5	Always available
MMC2_DIR_DAT1		O	Direction signal for DAT1..3 for use with external transceivers	Always available
MMC2_DAT6	P1-56*	IO	Card data bit 6	Always available
MMC2_DIR_CMD		O	Direction signal for CMD for use with external transceivers	Always available
MMC2_DAT7	P1-45*	IO	Card data bit 7	Only available **without** 'W' option
MMC2_CLKIN		I	Clock input signal for use with external transceivers	Only available **without** 'W' option
MMC-3				
MMC3_CLK	P1-123*	IO	MMC3 Interface clock	Only available **without** 'U' option
MMC3_CMD	P1-125*	O	Command signal	Only available **without** 'U' option
MMC3_DAT0	P1-120*	IO	Card data bit 0	Only available **without** 'U' option
	P1-54*			Only available **without** 'W' option
MMC3_DAT1	P1-124*	IO	Card data bit 1	Only available **without** 'U' option
	P1-39*			Always available
MMC3_DAT2	P1-126*	IO	Card data bit 2	Only available **without** 'U' option
	P1-56*			Always available
MMC3_DAT3	P1-45*	IO	Card data bit 3	Only available **without** 'W' option

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.11 Touch-Screen

The CM-T3730 features a resistive touch-screen interface. The interface supports 4-wire touch panels.

Table 22 Touch-screen signals

Signal Name	Pin #	Type	Description	Availability
TS_X+	P1-53	AIO	Touch screen X+ (right)	Only available **with** 'I' option.
TS_X-	P1-57	AIO	Touch screen X- (left)	Only available **with** 'I' option.
TS_Y+	P2-71	AIO	Touch screen Y+ (top)	Only available **with** 'I' option.
TS_Y-	P2-73	AIO	Touch screen Y- (bottom)	Only available **with** 'I' option.

4.12 Keypad

The CM-T3730 features a 6x6 matrix keypad interface derived from the keypad controller of the TI TPS65930 companion chip. The keypad controller implements a built-in scanning algorithm to decode hardware-based key presses and to reduce software overhead.

Figure 3 Keypad connection

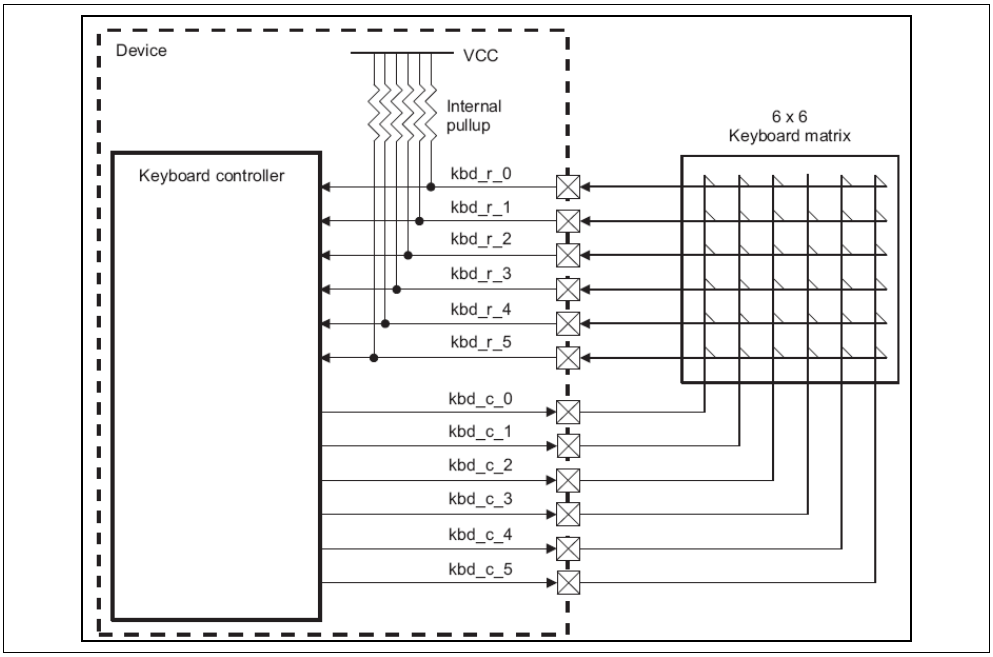


Table 23 Keypad signals

Signal Name	Pin #	Type	Description	Availability
KPD_R0	P2-48	I	Matrix key row input 0	Always available
KPD_R1	P2-52	I	Matrix key row input 1	Always available
KPD_R2	P2-54	I	Matrix key row input 2	Always available
KPD_R3	P2-56	I	Matrix key row input 3	Always available
KPD_R4	P2-58	I	Matrix key row input 4	Always available
KPD_R5	P2-60	I	Matrix key row input 5	Always available
KPD_C0	P2-53	OD, PU18	Matrix key column scan output 0	Always available
KPD_C1	P2-57	OD, PU18	Matrix key column scan output 1	Always available
KPD_C2	P2-59	OD, PU18	Matrix key column scan output 2	Always available
KPD_C3	P2-61	OD, PU18	Matrix key column scan output 3	Always available
KPD_C4	P2-63	OD, PU18	Matrix key column scan output 4	Always available
KPD_C5	P2-65	OD, PU18	Matrix key column scan output 5	Always available

4.13 GPIO

The CM-T3730 provides up to 104 GPIO signals. These signals can be configured for the following applications:

- Data input / output
- Keyboard interface with a debounce cell
- Interrupt generation
- Wake-up request

For additional details, please refer to section 25 of the "AM/DM37x Technical Reference Manual".

NOTE: Some GPIO signals can be used only as inputs, please note the GPIO signal type.

Table 24 GPIO availability

Signal name	Pin #	Type	Availability
GPIO_10	P1-133*	IO	Always available
GPIO_11	P2-18*	IO, PU18	Always available
GPIO_12	P1-123*	IO	Only available **without** 'U' option
GPIO_13	P1-125*	IO	Only available **without** 'U' option
GPIO_14	P1-128*	IO	Only available **without** 'U' option
GPIO_15	P1-119*	IO	Only available **without** 'U' option
GPIO_16	P1-130*	IO	Only available **without** 'U' option
GPIO_18	P1-120*	IO	Only available **without** 'U' option
GPIO_19	P1-124*	IO	Only available **without** 'U' option
GPIO_20	P1-126*	IO	Only available **without** 'U' option
GPIO_21	P1-121*	IO	Only available **without** 'U' option
GPIO_23	P1-117*	IO	Only available **without** 'U' option
GPIO_31	P2-20*	IO, PU18	Always available
GPIO_34	P1-71*	IO	Only available **without** 'E' option
GPIO_35	P1-70*	IO	Only available **without** 'E' option
GPIO_36	P1-73*	IO	Only available **without** 'E' option
GPIO_37	P1-72*	IO	Only available **without** 'E' option
GPIO_38	P1-75*	IO	Only available **without** 'E' option
GPIO_39	P1-76*	IO	Only available **without** 'E' option
GPIO_40	P1-77*	IO	Only available **without** 'E' option
GPIO_41	P1-78*	IO	Always available
GPIO_42	P1-81*	IO	Always available
GPIO_43	P1-80*	IO	Only available **without** 'E' option
GPIO_44	P1-104*	IO	Only available **without** 'E' option
GPIO_45	P1-105*	IO	Only available **without** 'E' option
GPIO_46	P1-106*	IO	Only available **without** 'E' option
GPIO_47	P1-107*	IO	Only available **without** 'E' option
GPIO_48	P1-108*	IO	Only available **without** 'E' option
GPIO_49	P1-109*	IO	Only available **without** 'E' option
GPIO_50	P1-112*	IO	Only available **without** 'E' option
GPIO_51	P1-111*	IO	Only available **without** 'E' option
GPIO_54	P1-92*	IO	Always available
GPIO_55	P1-93*	IO	Always available
GPIO_58	P1-85*	IO	Always available
GPIO_59	P1-88*	IO	Always available
GPIO_60	P1-82*	IO	Always available
GPIO_61	P1-87*	IO	Always available
GPIO_65	P1-83*	IO	Always available
GPIO_70	P1-58*	IO	Only available **without** 'W' option.
GPIO_71	P1-68*	IO	Only available **without** 'W' option.
GPIO_72	P1-113*	IO	Only available **without** 'W' option.
GPIO_73	P1-118*	IO	Only available **without** 'W' option.
GPIO_74	P1-129*	IO	Always available
GPIO_75	P2-64*	IO	Always available

Signal name	Pin #	Type	Availability
GPIO_94	P2-80*	IO	Always available
GPIO_95	P2-68*	IO	Always available
GPIO_96	P2-72*	IO	Always available
GPIO_97	P2-77*	IO	Always available
GPIO_98	P2-78*	IO	Always available
GPIO_99	P2-81*	I	Always available, Input only.
GPIO_100	P2-82*	I	Always available, Input only.
GPIO_101	P2-83*	IO	Always available
GPIO_102	P2-84*	IO	Always available
GPIO_103	P2-85*	IO	Always available
GPIO_104	P2-88*	IO	Always available
GPIO_105	P2-87*	I	Always available, Input only.
GPIO_106	P2-90*	I	Always available, Input only.
GPIO_107	P2-89*	I	Always available, Input only.
GPIO_108	P2-92*	I	Always available, Input only.
GPIO_109	P2-69*	IO	Always available
GPIO_110	P2-66*	IO	Always available
GPIO_111	P2-76*	IO	Always available
GPIO_120	P1-12*	O PUMMC	• Only available **without** 'NS8G' & 'NS0G' options • These pins MUST be left floating when CM-T3730 is configured for NS8G or NS0G options. • These pins are not available with CM-T3730 board revisions < 1.2
GPIO_121	P1-13*	IO PUMMC	
GPIO_122	P1-15*	IO PUMMC	
GPIO_123	P1-16*	IO PUMMC	
GPIO_124	P2-4*	IO PUMMC	
GPIO_125	P1-18*	IO PUMMC	
GPIO_130	P1-48*	IO	Only available **without** 'W' option.
GPIO_131	P1-41*	IO	Only available **without** 'W' option.
GPIO_132	P1-46*	IO	Only available **without** 'W' option.
GPIO_133	P1-47*	IO	Only available **without** 'W' option.
GPIO_134	P1-52*	IO	Only available **without** 'W' option.
GPIO_135	P1-49*	IO	Only available **without** 'W' option.
GPIO_136	P1-54*	IO	Only available **without** 'W' option
GPIO_137	P1-39*	IO	Always available
GPIO_138	P1-56*	IO	Always available
GPIO_139	P1-45*	IO	Only available **without** 'W' option.
GPIO_140	P1-33*	IO	Only available **without** 'W' option.
GPIO_141	P1-35*	IO	Only available **without** 'W' option.
GPIO_142	P1-32*	IO	Only available **without** 'W' option.
GPIO_143	P1-34*	IO	Only available **without** 'W' option.
GPIO_148	P1-24*	IO	Always available
GPIO_149	P1-29*	IO	Always available
GPIO_150	P1-27*	IO	Always available
GPIO_151	P1-22*	IO	Always available
GPIO_156	P2-28*	IO	Always available
GPIO_157	P2-30*	IO	Always available
GPIO_158	P2-32*	IO	Always available
GPIO_159	P2-34*	IO	Always available
GPIO_161	P2-27*	IO	Always available
GPIO_162	P2-29*	IO	Always available
GPIO_164	P1-42*	IO	Always available
GPIO_167	P2-70*	IO	Always available
GPIO_168	P1-61*	IO, PU18	Always available
GPIO_170	P1-36*	IO	Always available
GPIO_178	P2-45*	IO	Only available **without** 'U' option
GPIO_179	P2-39*	IO	Only available **without** 'U' option
GPIO_180	P2-49*	IO	Only available **without** 'U' option
GPIO_181	P2-47*	IO	Only available **without** 'U' option
GPIO_182	P2-37*	IO	Only available **without** 'U' option
GPIO_183	P1-60*	IO, PU18	Always available
GPIO_184	P1-63*	IO, PU18	Always available
GPIO_185	P1-64*	IO, PU18	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.14 Camera Interface

The camera interface is implemented with the camera sub-system (ISP) of the AM/DM37xx SoC. The camera ISP provides the system interface and the processing capability to connect RAW image-sensor modules to the CM-T3730. For additional details, please refer to section 6 of the "AM/DM37x Technical Reference Manual".

Table 25 Camera interface signals

Signal Name	Pin #	Type	Description	Availability
CAM_PCLK	P2-77*	I	Parallel interface pixel clock	Always available
CAM_HS	P2-80*	IO	Line trigger input/output signal	Always available
CAM_VS	P2-68*	IO	Frame trigger input/output signal	Always available
CAM_STROBE	P2-75	O	Flash strobe control signal	Always available
CAM_FLD	P2-78*	IO	Field identification input/output signal	Always available
CAM_GL_RST	P2-78*	IO	Camera global reset signal	Always available
	P1-39*			Always available
	P2-30*			Always available
CAM_SHUTTER	P1-56*	O	Camera shutter control signal.	Always available
	P2-70*			Always available
CAM_WEN	P2-70*	I	External write-enable signal	Always available
CAM_XCLKA	P2-72*	O	External clock for the image-sensor module	Always available
CAM_XCLKB	P2-76*	O	External clock for the image-sensor module	Always available
CAM_D0	P2-81*	I	Parallel input data line 0	Always available
CAM_D1	P2-82*	I	Parallel input data line 1	Always available
CAM_D2	P2-83*	I	Parallel input data line 2	Always available
CAM_D3	P2-84*	I	Parallel input data line 3	Always available
CAM_D4	P2-85*	I	Parallel input data line 4	Always available
CAM_D5	P2-88*	I	Parallel input data line 5	Always available
CAM_D6	P2-87*	I	Parallel input data line 6	Always available
CAM_D7	P2-90*	I	Parallel input data line 7	Always available
CAM_D8	P2-89*	I	Parallel input data line 8	Always available
CAM_D9	P2-92*	I	Parallel input data line 9	Always available
CAM_D10	P2-69*	I	Parallel input data line 10	Always available
CAM_D11	P2-66*	I	Parallel input data line 11	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.15 I²C

The CM-T3730 features two general purpose high speed I²C interfaces. The following features are supported:

- Compliance with Philips I²C specification version 2.1
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Support for HS mode for transfer up to 3.4M bits/s

Each of I2C interfaces may be used as a CAMERA management interface in conjunction with the SCCBE signal

The I²C interfaces are implemented with the I²C-2 and I²C-3 controller modules of the AM/DM37x SoC.

Table 26 I²C signals

Signal Name	Pin #	Type	Description
I²C-2			
I2C2_SDA	P1-60*	IOD, PU18	I2C serial data line
I2C2_SCL	P1-61*	OD, PU18	I2C serial clock line
I2C2_SCCBE	P1-36*	OD	Serial camera on I2C2 control bus enable signal
I²C-3			
I2C3_SDA	P1-64	IOD, PU18	I2C serial data line
I2C3_SCL	P1-63	OD, PU18	I2C serial clock line
I2C3_SCCBE	P1-36*	OD	Serial camera on I2C3 control bus enable signal

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.16 SPI

CM-T3730 features three multi-channel serial port interfaces (SPI). The following main features are supported:

- Serial clock with programmable frequency, polarity and phase for each channel
- A wide selection of SPI word lengths ranging from 4 bits to 32 bits

Table 27 SPI signals

Signal Name	Pin #	Type	Description	Availability
SPI-2				
SPI2_CLK	P2-45*	IO	Serial clock	Only available **without** 'U' option
SPI2_CS0	P2-47*	IO	Chip select 0	Only available **without** 'U' option
SPI2_CS1	P2-37*	O	Chip select 1	Only available **without** 'U' option
SPI2_SIMO	P2-39*	IO	Serial data master out	Only available **without** 'U' option
SPI2_SOMI	P2-49*	IO	Serial data master input	Only available **without** 'U' option
SPI-3				
SPI3_CLK	P1-48*	IO	Serial clock	Only available **without** 'W' option
SPI3_CS0	P1-49*	IO	Chip select 0	Only available **without** 'W' option
	P1-130*			Only available **without** 'U' option
SPI3_CS1	P1-52*	O	Chip select 1	Only available **without** 'W' option
	P1-121*			Only available **without** 'U' option
SPI3_SIMO	P1-41*	IO	Serial data master out	Only available **without** 'W' option
	P1-128*			Only available **without** 'U' option
SPI3_SOMI	P1-46*	IO	Serial data master input	Only available **without** 'W' option
	P1-119*			Only available **without** 'U' option

SPI-4				
SPI4_CLK	P2-28* P1-22*	IO	Serial clock	Always available
SPI4_CS0	P2-27*	IO	Chip select 0	Always available
SPI4_SIMO	P2-32*	IO	Serial data master out	Always available
SPI4_SOMI	P2-34*	IO	Serial data master input	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.17 McBSP

The CM-T3730 features three multi-channel buffered serial port (McBSP) interfaces. The following main features are supported:

- L4 interconnect slave interface supporting:
  - 32-bit data bus width
  - 32-bit access supported
  - 16- /8-bit access not supported
  - 10-bit address bus width
  - Write non-posted transaction mode supported
- 128 x 32-bit words (512 bytes) for each buffer for transmit/receive operations
- Interrupts configurable in legacy mode (2 requests) or PRCM compliant (1 request)
- Transmit and receive DMA requests triggered with programmable FIFO thresholds

For additional details, please refer to section 21 of the "AM/DM37x Technical Reference Manual".

Table 28 McBSP signals

Signal Name	Pin #	Type	Description	Availability
McBSP-1				
McBSP1_DR	P2-34*	I	Received serial data	Always available
McBSP1_CLKR	P2-28*	IO	Receive Clock	Always available
	P1-22*			Always available
McBSP1_FSR	P2-30*	IO	Receive frame synchronization	Always available
McBSP1_DX	P2-32*	O	Transmitted serial data	Always available
McBSP1_CLKX	P2-29*	IO	Transmit clock	Always available
McBSP1_FSX	P2-27*	IO	Transmit frame synchronization	Always available
McBSP-3				
McBSP3_DR	P1-35*	I	Received serial data	Only available **without** 'W' option
	P2-34*			Always available
McBSP3_DX	P1-33*	O	Transmitted serial data	Only available **without** 'W' option
	P2-32*			Always available
McBSP3_CLKX	P1-32*	IO	Transmit clock	Only available **without** 'W' option
	P2-29*			Always available
McBSP3_FSX	P1-34*	IO	Transmit frame synchronization	Only available **without** 'W' option
	P2-27*			Always available
McBSP-5				
McBSP5_DR	P1-120	I	Received serial data	Only available **without** 'U' option
McBSP5_DX	P1-126	O	Transmitted serial data	Only available **without** 'U' option
McBSP5_CLKX	P1-123	IO	Transmit clock	Only available **without** 'U' option
McBSP5_FSX	P1-124	IO	Transmit frame synchronization	Only available **without** 'U' option

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.18 HDQ / 1-Wire

The HDQ/1-Wire interface implements the hardware protocol of the master functions of the Benchmark HDQ and the Dallas Semiconductor 1-Wire® protocols.

The following main features are supported:

- Benchmark HDQ protocol
- Dallas Semiconductor 1-Wire® protocol
- Power-down mode

Table 29 HDQ / 1-Wire signals

Signal Name	Pin #	Type	Description	Availability
HDQ_SIO	P1-36*	OD	Serial data input/output	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.19 General Purpose Times and PWM

CM-T3730 has 11 general purpose timers GPTIMER1..GPTIMER11. The following features are supported

- Free-running 32-bit upward counter
- Programmable divider clock source
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- On-the-fly read/write register (while counting)
- 1-ms tick with 32,768 Hz functional clock generated (only GPTIMER10)

Timers 1..7 are not available at the CM-T3730 baseboard interface, and are used inside the CM-T3730 board. Timers 8..11 are available at the baseboard interface

For additional details, please refer to section 16 of the "AM/DM37x Technical Reference Manual".

Table 30 GPTIMERS and PWM signals

Signal Name	Pin #	Type	Description	Availability
GPT_8_PWM_EVT	P2-37* P1-85*	IO	GPTIMER8 trigger input/PWM output	Only available **without** 'U' option Always available
GPT_9_PWM_EVT	P2-39* P1-93*	IO	GPTIMER9 trigger input/PWM output	Only available **without** 'U' option Always available
GPT_10_PWM_EVT	P2-49*	IO	GPTIMER10 trigger input/PWM output	Only available **without** 'U' option
GPT_11_PWM_EVT	P2-47*	IO	GPTIMER11 trigger input/PWM output	Only available **without** 'U' option
SYS_CLKOUT1	P1-133*	O	Configurable output clock1. Can output main oscillator clock (26MHz)	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

4.20 Vibrator Driver

CM-T3730 provides a way to drive an external vibrator. The vibrator driver is based on the TI TPS65930 companion chip.

CM-T3730 vibrator driver supports the following main features:

- Audio signal driven vibration
- PWM controlled Vibration.

For additional details, please refer to section 10 of the "TPS65930 Technical Reference Manual".

Table 31 Vibrator signals

Signal Name	Pin #	Type	Description	Availability
VIBRA.P	P2-13*	OD	Vibrator driver positive	Always available
VIBRA.M	P2-15*	OD	Vibrator driver negative	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 2.2 of "TPS65930 Data Manual".

4.21 LED Drivers

The CM-T3730 features two open-drain LED drivers capable of driving two arrays of parallel LED's. These outputs are derived from the TPS65930 LED driver block.

For additional details, please refer to section 7 of the "TPS65930 Technical Reference Manual".

Table 32 Vibrator signals

Signal Name	Pin #	Type	Description	Availability
PMIC_LED_A	P2-13*	OD	PMIC LED A driver	Always available
PMIC_LED_B	P2-15*	OD	PMIC LED B driver	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 2.2 of "TPS65930 Data Manual".

4.22 ADC

The CM-T3730 features two general purpose ADC inputs implemented with the TPS65930 ADC block.

For additional details, please refer to section 8 of the "TPS65930 Technical Reference Manual".

Table 33 Miscellaneous signals

Signal Name	Pin #	Type	Description	Availability
ADC_IN0	P1-132	IO	General purpose ADC input 0.	Always available
ADC_IN2	P1-131	I	General purpose ADC input 2.	Always available

4.23 JTAG

The CM-T3730 JTAG interface is derived from the AM/DM37xx SoC JTAG port.

The AM/DM37xx target debug interface uses the five standard IEEE 1149.1 (JTAG) signals (nTRST, TCK, TMS, TDI and TDO), a return clock (RTCK) to meet the clocking requirements of the ARM968 processor and the two instrumentations pins (EMU0 and EMU1).

For additional details, please refer to section 26.6 of the "AM/DM37x Technical Reference Manual".

Table 34 JTAG signals

Signal Name	Pin #	Type	Description	Availability
JTAG_TCK	P2-24	I, PU18	Test clock	Always available
JTAG_TDO	P2-17	O, PU18	Test data output	Always available
JTAG_TDI	P2-21	I, PU18	Test data input	Always available
JTAG_TMS_TMSC	P2-23	IO, PU18	Test mode select	Always available
JTAG_nTRST	P2-25	I, PD	Test logic reset	Always available
JTAG_RTCK	P2-22	O, PU18	Returned test clock,	Always available
JTAG_EMU0	P2-18*	IO, PU18	Channel 0 trigger	Always available
JTAG_EMU1	P2-20*	IO, PU18	Channel 1 trigger	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

5 SYSTEM LOGIC

CM-T3730 implements a number of peripheral interfaces through the baseboard interface connectors (P1 and P2). The following notes apply to those interfaces:

- Some interfaces/signals are available only with/without certain configuration options of the CM-T3730. Each signal's availability is noted in the "Signals description" table of each interface.
- Most baseboard interface pins can be configured as one of several signals. For pin multiplexing characteristics, please refer to chapter 5.7.
- Certain signals are available on more than one baseboard interface pin. Only one pin can be used for each signal.
- All of the CM-T3730 digital interfaces operate at 1.8V voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" tables. The following notes summarize the column headers for these tables:

- **"Signal name"** – The symbolic name of each signal
- **"Pin#" –** The pin number on the baseboard interface connectors
- **"Type" –** Signal type
- **"Description" –** Signal description
- **"Availability" –** Certain signals are not available with/without certain configuration options. This column summarizes configuration requirements for each signal.

Each baseboard interface signal can be one of the following types. Signal type is noted in the "Signal description" tables for each signal

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"OD"** – Open Drain Signal (not pulled up onboard CM-T3730 unless otherwise noted).
- **"P"** – Power
- **"PU18"** – Always pulled up to 1.8V onboard CM-T3730
- **"PU33**" – Always pulled up to 3.3V onboard CM-T3730
- **"PUVCC"** – Always pulled up to VCC_CM onboard CM-T3730
- **"PD" -** Always pulled down onboard CM-T3730

5.1 Power Management

5.1.1 Power Rails

The CM-T3730 supports two power supply options:

- Regulated DC 3.8V
- Lithium-ion polymer battery

The CM-T3730 does not feature an onboard Lithium-ion polymer battery charger. If required, such a charger must be implemented on the baseboard.

Table 35 Power signals

Signal Name	Type	Description
VCC_CM	P	Main power supply. Typical voltage – 3.8V.
LCD_VIO	P	Power supply input for LCD interface. Connect to 1.8V / 2.5V / 3.3V power rail. The power source must provide 150mA continuous current.
BKBAT	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Leave unconnected if RTC back-up is not required.
GND	P	Common ground.

5.2 Reset

A full system reset, cold reset, is generated at power up by the TPS65930 companion chip to reset the full logic of the CM-T3730. Cold reset is a global reset that affects every module on the device. nRST_IN assertion also causes SYS_nRESWARM assertion.

The nRST_IN signal should be used as the main system reset.

For additional details, please refer to section 3 of the "AM/DM37x Technical Reference Manual".

Table 36 Reset signals

Signal Name	Pin #	Type	Description	Availability
nRST_IN	P1-11	IOD, PU18	Cold reset. Active low	Always available
SYS_nRESWARM	P1-116	IOD, PU18	Active low reset signal, triggered by asserting cold reset	Always available

5.3 Boot Sequence

The CM-T3730 standard boot sequence provides the following boot options:

- Boot from onboard micro-SD card
- Boot from external PC host via USB OTG port
- Boot from external PC host via RS232 port

The standard boot sequence is designed for normal system operation with the onboard micro-SD card as the boot media.

For additional details, please refer to section 25 of the "AM/DM37x Technical Reference Manual".

Table 37 CM-T3730 Boot sequence

First device	Second device	Third device
USB	RS232	MMC-1

5.4 System and Miscellaneous Signals

5.4.1 External DMA Requests

CM-T3730 provides up to four optional external DMA request signals that can be used by external devices to establish direct hardware synchronization with the AM/DM37x SDMA controller. A logical channel can be configured to respond to an external synchronization request.

For additional details, please refer to section 11 of the "AM/DM37x Technical Reference Manual".

Table 38 System signals

Signal Name	Pin #	Type	Description	Availability
nDMAREQ0	P1-92*	I	External DMA request 0	Always available
nDMAREQ1	P1-93*	I	External DMA request 1	Always available
	P1-83*			Always available
nDMAREQ2	P1-81*	I	External DMA request 2	Always available
nDMAREQ3	P1-80*	I	External DMA request 3	Only available **without** 'E' option

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.7 of this document.

5.5 External regulator control

CM-T3730 supports baseboard power supply control by means of a dedicated control signal. The external power supply control signal, EXT_REG_EN, is derived from the TI TPS65930 companion chip. Software can assert the EXT_REG_EN signal to shut down most baseboard power supplies when system is in low power mode.

For additional details, please refer to the "TPS65930 Technical Reference Manual".

Table 39 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
EXT_REG_EN	P2-12	O.D. PUVCC	baseboard power supply control signal (active high).	Always available

NOTE: EXT_REG_EN (active high) must be asserted when system is in normal operation mode.

5.6 Reserved Signals

CM-T3730 has several baseboard pins marked as reserved.

Reserved pins should be left un-connected. Connecting these pins may permanently damage the CM-T3730 board. The table below summarizes reserved pins.

Table 40 Reserved signals

Signal Name	Pin #	Type	Description	Availability
RESERVED1	P1-65	N.A.	Reserved pin, leave unconnected	Always available
RESERVED2	P1-66	N.A.	Reserved pin, leave unconnected	Always available
RESERVED3	P1-135	N.A.	Reserved pin, leave unconnected	Always available
RESERVED4	P2-10	N.A.	Reserved pin, leave unconnected	Always available

5.7 Signal Multiplexing Characteristics

AM/DM37x pins can have up to eight alternate function modes. The table below provides a description of signal multiplexing. Function names marked with gray shading denote the default function intended in the CM-T3730 design.

Table 41 Signal multiplexing

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P1-12	mmc1_clk	-	-	-	gpio_120	-	-	safe_mode
P1-13	mmc1_cmd	-	-	-	gpio_121	-	-	safe_mode
P1-15	mmc1_dat0	-	-	-	gpio_122	-	-	safe_mode
P1-16	mmc1_dat1	-	-	-	gpio_123	-	-	safe_mode
P1-18	mmc1_dat3	-	-	-	gpio_125	-	-	safe_mode
P1-22	uart1_rx	-	mcbsp1_clkr	mcspi4_clk	gpio_151	-	-	safe_mode
P1-24	uart1_tx	-	-	-	gpio_148	-	-	safe_mode
P1-27	uart1_cts	-	-	-	gpio_150	-	-	safe_mode
P1-29	uart1_rts	-	-	-	gpio_149	-	-	safe_mode
P1-32	mcbsp3_clkx	uart2_tx	-	-	gpio_142	-	-	safe_mode
P1-33	mcbsp3_dx	uart2_cts	-	-	gpio_140	-	-	safe_mode
P1-34	mcbsp3_fsx	uart2_rx	-	-	gpio_143	-	-	safe_mode
P1-35	mcbsp3_dr	uart2_rts	-	-	gpio_141	-	-	safe_mode
P1-36	hdq_sio	sys_altclk	i2c2_sccbe	i2c3_sccbe	gpio_170	-	-	safe_mode
P1-39	mmc2_dat5	mmc2_dir_dat1	cam_global_reset	mmc3_dat1	gpio_137	-	-	safe_mode
P1-41	mmc2_cmd	mcspi3_simo	-	-	gpio_131	-	-	safe_mode
P1-42	uart3_rts_sd	-	-	-	gpio_164	-	-	safe_mode
P1-45	mmc2_dat7	mmc2_clkin	-	mmc3_dat3	gpio_139	-	-	safe_mode
P1-46	mmc2_dat0	mcspi3_somi	-	-	gpio_132	-	-	safe_mode
P1-47	mmc2_dat1	-	-	-	gpio_133	-	-	safe_mode
P1-48	mmc2_clk	mcspi3_clk	-	-	gpio_130	-	-	safe_mode
P1-49	mmc2_dat3	mcspi3_cs0	-	-	gpio_135	-	-	safe_mode
P1-52	mmc2_dat2	mcspi3_cs1	-	-	gpio_134	-	-	safe_mode
P1-54	mmc2_dat4	mmc2_dir_dat0	-	mmc3_dat0	gpio_136	-	-	safe_mode
P1-56	mmc2_dat6	mmc2_dir_cmd	cam_shutter	mmc3_dat2	gpio_138	-	-	safe_mode
P1-58	dss_data0	-	uart1_cts	-	gpio_70	-	-	safe_mode
P1-60	i2c2_sda	-	-	-	gpio_183	-	-	safe_mode
P1-61	i2c2_scl	-	-	-	gpio_168	-	-	safe_mode
P1-63	i2c3_scl	-	-	-	gpio_184	-	-	safe_mode
P1-64	i2c3_sda	-	-	-	gpio_185	-	-	safe_mode
P1-68	dss_data1	-	uart1_rts	-	gpio_71	-	-	safe_mode
P1-70	gpmc_a2	-	-	-	gpio_35	-	-	safe_mode
P1-71	gpmc_a1	-	-	-	gpio_34	-	-	safe_mode
P1-72	gpmc_a4	-	-	-	gpio_37	-	-	safe_mode
P1-73	gpmc_a3	-	-	-	gpio_36	-	-	safe_mode
P1-75	gpmc_a5	-	-	-	gpio_38	-	-	safe_mode
P1-76	gpmc_a6	-	-	-	gpio_39	-	-	safe_mode
P1-77	gpmc_a7	-	-	-	gpio_40	-	-	safe_mode
P1-78	gpmc_a8	-	-	-	gpio_41	-	-	safe_mode
P1-80	gpmc_a10	sys_ndmareq3	-	-	gpio_43	-	-	safe_mode
P1-81	gpmc_a9	sys_ndmareq2	-	-	gpio_42	-	-	safe_mode
P1-82	gpmc_nbe0_cle	-	-	-	gpio_60	-	-	safe_mode
P1-83	gpmc_wait3	sys_ndmareq1	-	-	gpio_65	-	-	safe_mode
P1-85	gpmc_ncs7	gpmc_io_dir	mcbsp4_fsx	gpt8_pwm_evt	gpio_58	-	-	
P1-87	gpmc_nbe1	-	-	-	gpio_61	-	-	safe_mode
P1-88	gpmc_clk	-	-	-	gpio_59	-	-	safe_mode
P1-92	gpmc_ncs3	sys_ndmareq0	-	-	gpio_54	-	-	safe_mode
P1-93	gpmc_ncs4	sys_ndmareq1	mcbsp4_clkx	gpt9_pwm_evt	gpio_55	-	-	safe_mode
P1-104	gpmc_d8	-	-	-	gpio_44	-	-	safe_mode
P1-105	gpmc_d9	-	-	-	gpio_45	-	-	safe_mode
P1-106	gpmc_d10	-	-	-	gpio_46	-	-	safe_mode
P1-107	gpmc_d11	-	-	-	gpio_47	-	-	safe_mode

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P1-108	gpmc_d12	-	-	-	gpio_48	-	-	safe_mode
P1-109	gpmc_d13	-	-	-	gpio_49	-	-	safe_mode
P1-111	gpmc_d15	-	-	-	gpio_51	-	-	safe_mode
P1-112	gpmc_d14	-	-	-	gpio_50	-	-	safe_mode
P1-113	dss_data2	-	-	-	gpio_72	-	-	safe_mode
P1-117	etk_d9	sys_secure_ indicator	mmc3_dat5	hsusb1_nxt	gpio_23	mm1_rxdm	hsusb1_tll _nxt	-
P1-118	dss_data3	-	-	-	gpio_73	-	-	safe_mode
P1-119	etk_d1	mcspi3_somi	-	hsusb1_data1	gpio_15	mm1_txse0	hsusb1_tll _data1	-
P1-120	etk_d4	mcbsp5_dr	mmc3_dat0	hsusb1_data4	gpio_18	-	hsusb1_tll _data4	-
P1-121	etk_d7	mcspi3_cs1	mmc3_dat7	hsusb1_data3	gpio_21	mm1_txen _n	hsusb1_tll _data3	-
P1-123	etk_clk	mcbsp5_clkx	mmc3_clk	hsusb1_stp	gpio_12	mm1_rxdp	hsusb1_tll _stp	-
P1-124	etk_d5	mcbsp5_fsx	mmc3_dat1	hsusb1_data5	gpio_19	-	hsusb1_tll _data5	-
P1-125	etk_ctl	-	mmc3_cmd	hsusb1_clk	gpio_13	-	hsusb1_tll _clk	-
P1-126	etk_d6	mcbsp5_dx	mmc3_dat2	hsusb1_data6	gpio_20	-	hsusb1_tll _data6	-
P1-128	etk_d0	mcspi3_simo	mmc3_dat4	hsusb1_data0	gpio_14	mm1_rxrcv	hsusb1_tll _data0	-
P1-129	dss_data4	-	uart3_rx_ irrx	-	gpio_74	-	-	safe_mode
P1-130	etk_d2	mcspi3_cs0	-	hsusb1_data2	gpio_16	mm1_txdat	hsusb1_tll _data2	-
P1-133	sys_clkout1	-	-	-	gpio_10	-	-	safe_mode
P2-4	mmc1_dat2	-	-	-	gpio_124	-	-	safe_mode
P2-18	jtag_emu0	-	-	-	gpio_11	-	-	safe_mode
P2-20	jtag_emu1	-	-	-	gpio_31	-	-	safe_mode
P2-27	mcbsp1_fsx	mcspi4_cs0	mcbsp3_fsx	-	gpio_161	-	-	safe_mode
P2-28	mcbsp1_clkr	mcspi4_clk	-	-	gpio_156	-	-	safe_mode
P2-29	mcbsp1_clkx	-	mcbsp3_clkx	-	gpio_162	-	-	safe_mode
P2-30	mcbsp1_fsr	-	cam_global _reset	-	gpio_157	-	-	safe_mode
P2-32	mcbsp1_dx	mcspi4_simo	mcbsp3_dx	-	gpio_158	-	-	safe_mode
P2-34	mcbsp1_dr	mcspi4_somi	mcbsp3_dr	-	gpio_159	-	-	safe_mode
P2-37	mcspi2_cs1	gpt8_pwm _evt	hsusb2_tll _data3	hsusb2_data3	gpio_182	mm2_txen _n	-	safe_mode
P2-39	mcspi2_simo	gpt9_pwm _evt	hsusb2_tll _data4	hsusb2_data4	gpio_179	-	-	safe_mode
P2-45	mcspi2_clk	-	hsusb2_tll _data7	hsusb2_data7	gpio_178	-	-	safe_mode
P2-47	mcspi2_cs0	gpt11_pwm _evt	hsusb2_tll _data6	hsusb2_data6	gpio_181	-	-	safe_mode
P2-49	mcspi2_somi	gpt10_pwm _evt	hsusb2_tll _data5	hsusb2_data5	gpio_180	-	-	safe_mode
P2-64	dss_data5	-	uart3_tx_ irtx	gpio_75	-	-	-	safe_mode
P2-66	cam_d11	-	-	-	gpio_110	-	-	safe_mode
P2-68	cam_vs	-	-	-	gpio_95	-	-	safe_mode
P2-69	cam_d10	-	-	-	gpio_109	-	-	safe_mode
P2-70	cam_wen	-	cam_shutter	-	gpio_167	-	-	safe_mode
P2-72	cam_xclka	-	-	-	gpio_96	-	-	safe_mode
P2-75	cam_strobe	-	-	-	gpio_126	-	-	safe_mode
P2-76	cam_xclkb	-	-	-	gpio_111	-	-	safe_mode
P2-77	cam_pclk	-	-	-	gpio_97	-	-	safe_mode
P2-78	cam_fld	-	cam_global _reset	-	gpio_98	-	-	safe_mode
P2-80	cam_hs	-	-	-	gpio_94	-	-	safe_mode
P2-81	cam_d0	-	-	-	gpio_99	-	-	safe_mode
P2-82	cam_d1	-	-	-	gpio_100	-	-	safe_mode
P2-83	cam_d2	-	-	-	gpio_101	-	-	safe_mode
P2-84	cam_d3	-	-	-	gpio_102	-	-	safe_mode
P2-85	cam_d4	-	-	-	gpio_103	-	-	safe_mode
P2-87	cam_d6	-	-	-	gpio_105	-	-	safe_mode

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P2-88	cam_d5	-	-	-	gpio_104	-	-	safe_mode
P2-89	cam_d8	-	-	-	gpio_107	-	-	safe_mode
P2-90	cam_d7	-	-	-	gpio_106	-	-	safe_mode
P2-92	cam_d9	-	-	-	gpio_108	-	-	safe_mode

5.8 RTC

The CM-T3730 RTC is implemented with the internal RTC of the TI TPS65930 companion chip. The RTC provides time and calendar information, timed interrupt generation and alarm wake-up event functionality.

Additionally, a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. If the backup battery is rechargeable, the device also provides a backup battery charger so it can be recharged when the main battery supply is present. The backup battery should be connected to the BKBAT power input.

For additional details, please refer to section 3 of the "TPS65930 Technical Reference Manual".

5.9 LED

The CM-T3730 features a single general purpose green LED controlled by GPIO186 of the AM/DM37xx SoC. The LED is ON when GPIO186 is set high.

6 BASEBOARD INTERFACE

The CM-T3730 connects to the baseboard through P1 and P2 - 0.6 mm pitch 140-pin connectors.

6.1 Connector Pinout

Table 42 Connector P1

Pin #	CM-T3730 Signal Name	Reference Section		Pin #	CM-T3730 Signal Name	Reference Section
P1-01	CM_ETH_TXP	4.3		P1-02	CM_ETH_RXN	4.3
P1-03	CM_ETH_TXN	4.3		P1-04	CM_ETH_RXP	4.3
P1-05	CM_ETH_LED2	4.3		P1-06	CM_ETH_LED1	4.3
P1-07	VCC_CM	5.1.1		P1-08	GND	5.1.1
P1-09	N.C.			P1-10	VCC_MMC	4.10
P1-11	nRST_IN	5.2		P1-12	MMC1_CLK GPIO120	4.10 4.13
P1-13	MMC1_CMD GPIO121	4.10 4.13		P1-14	GND	5.1.1
P1-15	MMC1_DAT0 GPIO122	4.10 4.13		P1-16	MMC1_DAT1 GPIODAT1	4.10 4.13
P1-17	N.C.			P1-18	MMC1_DAT3 GPIO125	4.10 4.13
P1-19	VCC_CM	5.1.1		P1-20	BKBAT	5.1.1
P1-21	N.C.			P1-22	UART1_RX McBSP1_CLKR SPI4_CLK GPIO151	4.7 4.17 4.16 4.13
P1-23	N.C.			P1-24	UART1_TX GPIO148	4.7 4.13
P1-25	N.C.			P1-26	GND	5.1.1
P1-27	UART1_CTS GPIO150	4.7 4.13		P1-28	RS232_RXD	4.8
P1-29	UART1_RTS GPIO149	4.7 4.13		P1-30	RS232_TXD	4.8
P1-31	VCC_CM	5.1.1		P1-32	McBSP3_CLKX UART2_TX GPIO142	4.17 4.7 4.13
P1-33	McBSP3_DX UART2_CTS GPIO140	4.17 4.7 4.13		P1-34	McBSP3_FSX UART2_RX GPIO143	4.17 4.7 4.13
P1-35	McBSP3_DR UART2_RTS GPIO141	4.17 4.7 4.13		P1-36	HDQ_SIO I2C2_SCCBE I2C3_SCCBE GPIO170	4.18 4.15 4.15 4.13
P1-37	N.C.			P1-38	GND	5.1.1
P1-39	MMC2_DAT5 MMC2_DIR_DAT1 CAM_GL_RST MMC3_DAT1 GPIO137	4.10 4.10 4.14 4.10 4.13		P1-40	N.C.	
P1-41	MMC2_CMD SPI3_SIMO GPIO131	4.10 4.16 4.13		P1-42	IRDA_SD GPIO164	4.9 4.13
P1-43	VCC_CM	5.1.1		P1-44	N.C.	
P1-45	MMC2_DAT7 MMC2_CLKIN MMC3_DAT3 GPIO139	4.10 4.10 4.10 4.13		P1-46	MMC2_DAT0 SPI3_SOMI GPIO132	4.10 4.16 4.13
P1-47	MMC2_DAT1 GPIO133	4.10 4.13		P1-48	MMC2_CLK SPI3_CLK GPIO130	4.10 4.16 4.13
P1-49	MMC2_DAT3 SPI3_CS0 GPIO135	4.10 4.16 4.13		P1-50	GND	5.1.1

Pin #	CM-T3730 Signal Name	Reference Section		Pin #	CM-T3730 Signal Name	Reference Section
P1-51	N.C.			P1-52	MMC2_DAT2 SPI3_CS1 GPIO134	4.10 4.16 4.13
P1-53	TS_X+	4.11		P1-54	MMC2_DAT4 MMC2_DIR_DAT0 MMC3_DAT0 GPIO136	4.10 4.10 4.10 4.13
P1-55	VCC_CM	5.1.1		P1-56	MMC2_DAT6 MMC2_DIR_CMD CAM_SHUTTER MMC3_DAT2 GPIO138	4.10 4.10 4.14 4.10 4.13
P1-57	TS_X-	4.11		P1-58	LCD_D0 UART1_CTS GPIO70	4.2 4.7 4.13
P1-59	N.C.			P1-60	I2C2_SDA GPIO183	4.15 4.13
P1-61	I2C2_SCL GPIO168	4.15 4.13		P1-62	GND	5.1.1
P1-63	I2C3_SCL GPIO184	4.15 4.13		P1-64	I2C3_SDA GPIO185	4.15 4.13
P1-65	RESERVED1	5.6		P1-66	RESERVED2	5.6
P1-67	VCC_CM	5.1.1		P1-68	LCD_D1 UART1_RTS GPIO71	4.2 4.7 4.13
P1-69	N.C.			P1-70	GPMC_A2 GPIO35	4.1 4.13
P1-71	GPMC_A1 GPIO34	4.1 4.13		P1-72	GPMC_A4 GPIO37	4.1 4.13
P1-73	GPMC_A3 GPIO36	4.1 4.13		P1-74	GND	5.1.1
P1-75	GPMC_A5 GPIO38	4.1 4.13		P1-76	GPMC_A6 GPIO39	4.1 4.13
P1-77	GPMC_A7 GPIO40	4.1 4.13		P1-78	GPMC_A8 GPIO41	4.1 4.13
P1-79	VCC_CM	5.1.1		P1-80	GPMC_A10 nDMAREQ3 GPIO43	4.1 5.4.1 4.13
P1-81	GPMC_A9 nDMAREQ2 GPIO43	4.1 5.4.1 4.13		P1-82	GPMC_nBE0 GPMC_CLE GPIO60	4.1 4.1 4.13
P1-83	GPMC_WAIT3 nDMAREQ1 GPIO65	4.1 5.4.1 4.13		P1-84	GPMC_nWE	4.1
P1-85	GPMC_nCS7 GPMC_IODIR GPT_8_PWM_EVT GPIO58	4.1 4.1 4.19 4.13		P1-86	GND	5.1.1
P1-87	GPMC_nBE1 GPIO61	4.1 4.13		P1-88	GPMC_CLK GPIO59	4.1 4.13
P1-89	GPMC_nOE	4.1		P1-90	GPMC_nADV GPMC_ALE	4.1 4.1
P1-91	VCC_CM	5.1.1		P1-92	GPMC_nCS3 nDMAREQ0 GPIO54	4.1 5.4.1 4.13
P1-93	GPMC_nCS4 nDMAREQ1 GPT_9_PWM_EVT GPIO55	4.1 5.4.1 4.19 4.13		P1-94	GPMC_D0	4.1
P1-95	GPMC_D1	4.1		P1-96	GPMC_D2	4.1
P1-97	GPMC_D3	4.1		P1-98	GND	5.1.1
P1-99	GPMC_D5	4.1		P1-100	GPMC_D4	4.1
P1-101	GPMC_D7	4.1		P1-102	GPMC_D6	4.1
P1-103	VCC_CM	5.1.1		P1-104	GPMC_D8 GPIO44	4.1 4.13
P1-105	GPMC_D9 GPIO45	4.1 4.13		P1-106	GPMC_D10 GPIO46	4.1 4.13

Pin #	CM-T3730 Signal Name	Reference Section		Pin #	CM-T3730 Signal Name	Reference Section
P1-107	GPMC_D11 GPIO47	4.1 4.13		P1-108	GPMC_D12 GPIO48	4.1 4.13
P1-109	GPMC_D13 GPIO49	4.1 4.13		P1-110	GND	5.1.1
P1-111	GPMC_D15 GPIO51	4.1 4.13		P1-112	GPMC_D14 GPIO50	4.1 4.13
P1-113	LCD_D2 GPIO72	4.2 4.13		P1-114	GND	5.1.1
P1-115	VCC_CM	5.1.1		P1-116	SYS_nRESWARM	5.2
P1-117	GPIO23	4.13		P1-118	LCD_D3 GPIO73	4.2 4.13
P1-119	SPI3_SOMI GPIO15	4.16 4.13		P1-120	McBSP5_DR MMC3_DAT0 GPIO18	4.17 4.10 4.13
P1-121	SPI3_CS1 GPIO21	4.16 4.13		P1-122	GND	5.1.1
P1-123	McBSP5_CLKX MMC3_CLK GPIO12	4.17 4.10 4.13		P1-124	McBSP5_FSX MMC3_DAT1 GPIO19	4.17 4.10 4.13
P1-125	MMC3_CMD GPIO13	4.10 4.13		P1-126	McBSP5_DX MMC3_DAT2 GPIO20	4.17 4.10 4.13
P1-127	VCC_CM	5.1.1		P1-128	SPI3_SIMO GPIO14	4.16 4.13
P1-129	LCD_D4 UART3_RX IRDA_RX GPIO74	4.2 4.7 4.9 4.13		P1-130	SPI3_CS0 GPIO16	4.16 4.13
P1-131	ADC_IN2	4.22		P1-132	ADC_IN0	4.22
P1-133	SYS_CLKOUT1 GPIO10	4.19 4.13		P1-134	GND	5.1.1
P1-135	RESERVED3	5.6		P1-136	USB0_DP	4.4.1
P1-137	USB0_ID	4.4.1		P1-138	USB0_DN	4.4.1
P1-139	VCC_CM	5.1.1		P1-140	USB0_5V_OUT	4.4.1

Table 43 Connector P2

Pin #	CM-T3730 Signal Name	Reference Section		Pin #	CM-T3730 Signal Name	Reference Section
P2-01	TV_OUT1	4.2		P2-02	GND	5.1.1
P2-03	TV_OUT2	4.2		P2-04	MMC1_DAT2 GPIO124	4.10 4.13
P2-05	N.C.			P2-06	USB1_CPEN	4.4.2
P2-07	VCC_CM	5.1.1		P2-08	USB1_VBUS	4.4.2
P2-09	USB2_CPEN	4.4.2		P2-10	RESERVED4	5.6
P2-11	USB2_VBUS	4.4.2		P2-12	EXT_REG_EN	5.5
P2-13	PMIC_LED_A VIBRA.P	4.21 4.20		P2-14	GND	5.1.1
P2-15	PMIC_LED_B VIBRA.M	4.21 4.20		P2-16	LCD_VIO	4.2
P2-17	JTAG_TDO	4.23		P2-18	JTAG_EMU0 GPIO11	4.23 4.13
P2-19	VCC_CM	5.1.1		P2-20	JTAG_EMU1 GPIO31	4.23 4.13
P2-21	JTAG_TDI	4.23		P2-22	JTAG_RTCK	4.23
P2-23	JTAG_TMS	4.23		P2-24	JTAG_TCK	4.23
P2-25	JTAG_nTRST	4.23		P2-26	GND	5.1.1
P2-27	McBSP1_FSX SPI4_CS0 McBSP3_FSX GPIO161	4.17 4.16 4.17 4.13		P2-28	McBSP1_CLKR SPI4_CLK GPIO156	4.17 4.16 4.13
P2-29	McBSP1_CLKX McBSP3_CLKX GPIO162	4.17 4.17 4.13		P2-30	McBSP1_FSR CAM_GL_RST GPIO157	4.17 4.16 4.13
P2-31	VCC_CM	5.1.1		P2-32	McBSP1_DX SPI4_SIMO McBSP3_DX GPIO158	4.17 4.16 4.17 4.13

Pin #	CM-T3730 Signal Name	Reference Section		Pin #	CM-T3730 Signal Name	Reference Section
P2-33	N.C.			P2-34	McBSP1_DR SPI4_SOMI McBSP3_DR GPIO159	4.17 4.16 4.17 4.13
P2-35	N.C.			P2-36	N.C.	
P2-37	SPI2_CS1 GPT_8_PWM_EVT GPIO182	4.16 4.19 4.13		P2-38	GND	5.1.1
P2-39	SPI2_SIMO GPT_9_PWM_EVT GPIO179	4.16 4.19 4.13		P2-40	N.C.	
P2-41	N.C.			P2-42	N.C.	
P2-43	VCC_CM	5.1.1		P2-44	N.C.	
P2-45	SPI2_CLK GPIO178	4.16 4.13		P2-46	N.C.	
P2-47	SPI2_CS0 GPT_11_PWM_EVT GPIO181	4.16 4.19 4.13		P2-48	KPD_R0	4.12
P2-49	SPI2_SOMI GPT_10_PWM_EVT GPIO180	4.16 4.19 4.13		P2-50	GND	5.1.1
P2-51	N.C			P2-52	KPD_R1	4.12
P2-53	KPD_C0	4.12		P2-54	KPD_R2	4.12
P2-55	VCC_CM	5.1.1		P2-56	KPD_R3	4.12
P2-57	KPD_C1	4.12		P2-58	KPD_R4	4.12
P2-59	KPD_C2	4.12		P2-60	KPD_R5	4.12
P2-61	KPD_C3	4.12		P2-62	GND	5.1.1
P2-63	KPD_C4	4.12		P2-64	LCD_D5 UART3_TX IRDA_TX GPIO75	4.2 4.7 4.9 4.13
P2-65	KPD_C5	4.12		P2-66	CAM_D11 GPIO110	4.14 4.13
P2-67	VCC_CM	5.1.1		P2-68	CAM_VS GPIO95	4.14 4.13
P2-69	CAM_D10 GPIO109	4.14 4.13		P2-70	CAM_WEN GPIO167	4.14 4.13
P2-71	TS_Y+	4.11		P2-72	CAM_XCLKA GPIO96	4.14 4.13
P2-73	TS_Y-	4.11		P2-74	GND	5.1.1
P2-75	CAM_STROBE GPIO126	4.14 4.13		P2-76	CAM_XCLKB GPIO111	4.14 4.13
P2-77	CAM_PCLK GPIO97	4.14 4.13		P2-78	CAM_FLD GPIO98	4.14 4.13
P2-79	VCC_CM	5.1.1		P2-80	CAM_HS GPIO94	4.14 4.13
P2-81	CAM_D0 GPIO99	4.14 4.13		P2-82	CAM_D1 GPIO100	4.14 4.13
P2-83	CAM_D2 GPIO101	4.14 4.13		P2-84	CAM_D3 GPIO102	4.14 4.13
P2-85	CAM_D4 GPIO103	4.14 4.13		P2-86	GND	5.1.1
P2-87	CAM_D6 GPIO105	4.14 4.13		P2-88	CAM_D5 GPIO104	4.14 4.13
P2-89	CAM_D8 GPIO107	4.14 4.13		P2-90	CAM_D7 GPIO106	4.14 4.13
P2-91	VCC_CM	5.1.1		P2-92	CAM_D9 GPIO108	4.14 4.13
P2-93	LCD_D23	4.2		P2-94	LCD_D22	4.2
P2-95	LCD_D0	4.2		P2-96	LCD_HSYNC	4.2
P2-97	LCD_D1	4.2		P2-98	GND	5.1.1
P2-99	LCD_D3	4.2		P2-100	LCD_D2	4.2
P2-101	LCD_D5	4.2		P2-102	LCD_D4	4.2
P2-103	VCC_CM	5.1.1		P2-104	LCD_D6	4.2
P2-105	LCD_D8	4.2		P2-106	LCD_D7	4.2
P2-107	LCD_D10	4.2		P2-108	LCD_D9	4.2
P2-109	LCD_D11	4.2		P2-110	GND	5.1.1
P2-111	LCD_VSYNC	4.2		P2-112	LCD_PCLK	4.2

Pin #	CM-T3730 Signal Name	Reference Section		Pin #	CM-T3730 Signal Name	Reference Section
P2-113	LCD_D12	4.2		P2-114	LCD_ACBIAS	4.2
P2-115	VCC_CM	5.1.1		P2-116	LCD_D13	4.2
P2-117	LCD_D15	4.2		P2-118	LCD_D14	4.2
P2-119	LCD_D17	4.2		P2-120	LCD_D16	4.2
P2-121	LCD_D19	4.2		P2-122	GND	5.1.1
P2-123	LCD_D21	4.2		P2-124	LCD_D18	4.2
P2-125	GND	5.1.1		P2-126	LCD_D20	4.2
P2-127	VCC_CM	5.1.1		P2-128	AUDIO_IN	0
P2-129	MIC_BIAS	0		P2-130	AUDIO_OUT_L	0
P2-131	MIC_IN_P	0		P2-132	GND	5.1.1
P2-133	MIC_IN_N	0		P2-134	GND	5.1.1
P2-135	VCC_CM	5.1.1		P2-136	AUDIO_OUT_R	0
P2-137	USB2_DP	4.4.2		P2-138	USB1_DP	4.4.2
P2-139	USB2_DM	4.4.2		P2-140	USB1_DM	4.4.2

6.2 Connector Type

Table 44 Connector type

Part Reference	Mfg.	CM-T3730 connector P/N	Baseboard (mating) connector P/N
P1, P2	AMP	1-5353183-0	1-5353190-0 or CON140

Mating connectors and standoffs are available from CompuLab, see [prices] >> [accessories] links at CompuLab's website.

CompuLab's P/N for the AMP 1-5353190-0 connector is "CON140".

6.3 Mechanical Drawings

Figure 4 CM-T3730 top

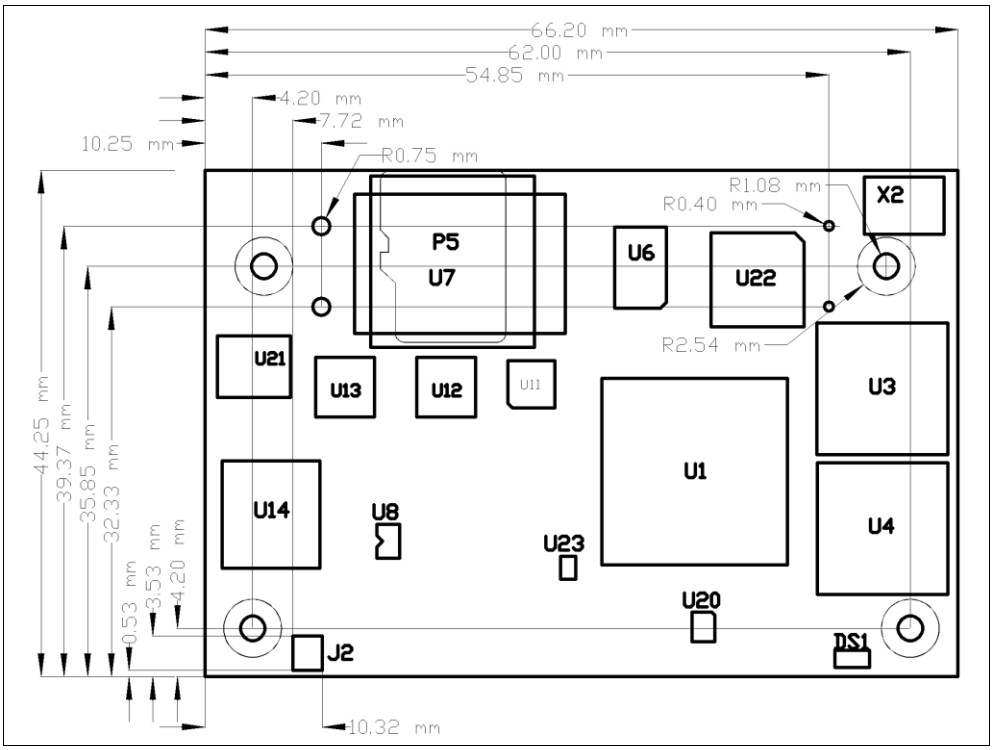
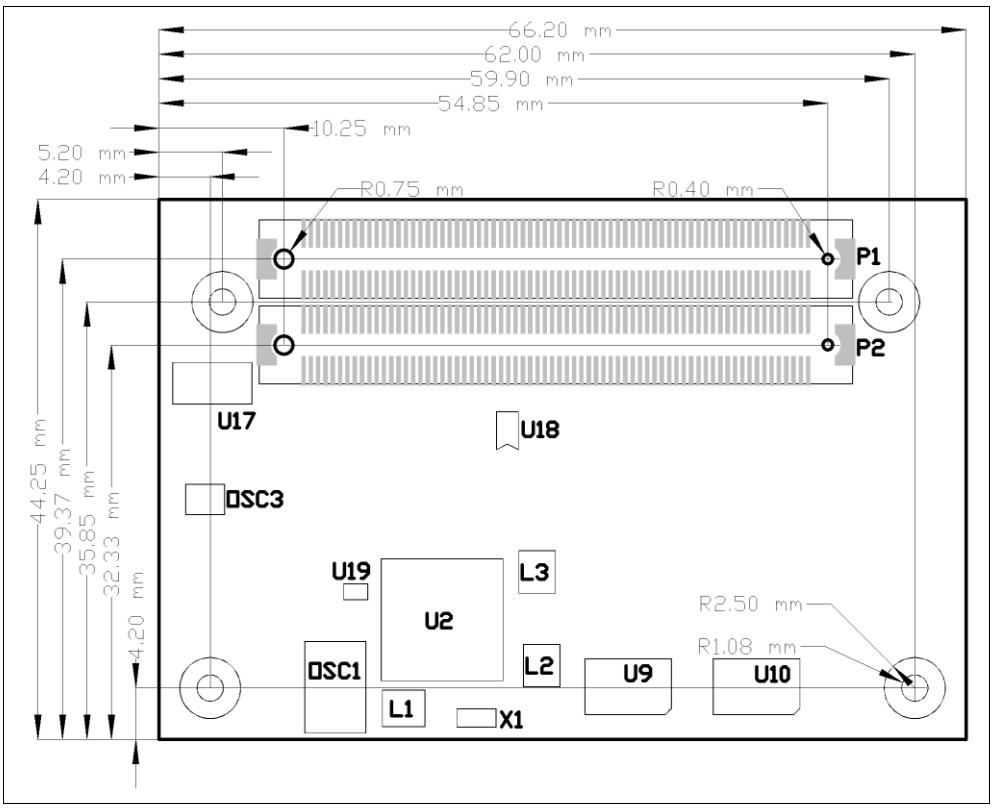


Figure 5 CM-T3730 bottom (X-Ray view - as seen from top side)



1. All dimensions are in millimeters.
2. Height of all components is <2mm.
3. Baseboard connectors provide 4mm board-to-board clearance.
4. Board thickness is 1.6mm.

Mechanical drawings are available for download in DXF format the CompuLab website, by opening the "Development Resources" tab of the CM-T3730 product page and downloading the "CM-T3730 dimensions and connector locations" file.

6.4 Standoffs

The CM-T3730 has four mounting holes for standoffs. Standoffs are implemented with three parts: screw, spacer and nut.

Table 45 Standoffs

Part	Description	Manufacturer and P/N
Screw	M2, 10 mm length	• FCI 95121-005 • Acton InoxPro BF22102010 • World Bridge Machinery 380J52080
Spacer	M2 x 4 thread, 4.2 mm length	• Hirosugi ASU-2004 • MAC8 2SP-4 • World Bridge Machinery M2, L=4.2 mm
Nut	M2, 1.6-2.0mm width	• FCI 92869-001 (or 002) • Acton InoxPro BG12102000 • Bossard 1241397 (DIN934-A2 M2) • World Bridge Machinery 381A52000

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 46 Absolute Maximum ratings

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VCC_CM)	Only without 'W' option	2.1		4.5	V
Main power supply voltage (VCC_CM)	with 'W' option	2.1		4.2	V
LCD interface power supply voltage (LCD_VIO)		-0.5		4.6	V

7.2 Recommended Operating Conditions

Table 47 Recommended Operating Conditions

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VCC_CM)	Only without 'W' option	3.4	3.8	4.5	V
Main power supply voltage (VCC_CM)	with 'W' option	3.4	3.8	4.2	V
LCD interface power supply voltage (LCD_VIO)		TBD	3.3	3.6	V
RTC backup battery voltage (BKBAT)		1.8	3.2	3.3	V

7.3 DC Electrical Characteristics

Table 48 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
1.8V Digital I/O					
V_{IH}		1.17		2.1	V
V_{IL}		-0.3		0.63	V
V_{OH}		1.4			V
V_{OL}				0.4	V
LCD Interface					
V_{OH}	LCD_VIO = 3.3V	2.3			V
					V
V_{OL}	LCD_VIO = 3.3V			0.7	V
					V
I^2C (open drain with internal pull up to 1.8V)					
V_{IH}		1.26		2.3	V
V_{IL}		-0.5		0.54	V
V_{OH} (open drain with 3mA sink current)		0		0.36	V
JTAG					
V_{IH}		1.17		2.1	V
V_{IL}		-0.3		0.63	V
V_{OH}		1.6			V
V_{OL}				0.2	V
RS232					
TX Voltage Swing		±5	±5.4		V
RX Voltage Swing			±25		V
EXT_REG_EN					
V_{OH}		VCC_CM-0.45		VCC_CM	V
V_{OL}		0		0.45	V

7.4 Power Output Characteristics

Table 49 Power Output Characteristics

Parameter	Min	Typ	Max	Unit
USB0_5V_OUT				
Output voltage		4.8		V
Rated output current		100		mA

7.5 ESD Performance

Table 50 ESD Performance

Interface	ESD Performance
USB OTG	±8 kV ESD using HBM
USB host	±8 kV ESD using HBM
RS232	±15 kV ESD using HBM

7.6 Operating Temperature Ranges

The CM-T3730 is available with three options of operating temperature range.

Table 51 CM-T3730 Temperature Range Options

Range	Temp.	Description
Commercial	0^{o} to 70^{o} C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20^{o} to 70^{o} C	Every board undergoes a short test for the lower limit (-20^{o} C) qualification.
Industrial	-40^{o} to 85^{o} C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Baseboard Design Guidelines

- Ensure that all VCC_CM and GND power pins are connected.
- Major power rails - VCC_CM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system's signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between VCC_CM and GND near the mating connectors.
- It is recommended to connect the standoff holes of the baseboard to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CM-T3730 operation. All power-up circuitry and all required pullups/pulldowns are found on the module.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIO's), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet and USB signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of baseboard noise.
  - Local bus signals must be buffered in most cases.
- Be careful when placing components under the CM-T3730 module. The baseboard interface connector provides 4mm mating height. Bear in mind that there are components on the underside of the CM-T3730. Maximum allowable height for components placed under the CM-T3730 is 1.5mm.
- Refer to the SB-T35 baseboard reference design schematics.

8.2 Baseboard Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the baseboard. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the VCC_CM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:

- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module's on-board values, or any other component creating the same "overriding" effect
- Faulty power supply

- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the baseboard, shorting them on the connectors can disable the module's operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector's body. Note that solder shorts are the most frequent factor disabling a module's start.
- Check possible signal's shorting due to errors of baseboard PCB design or assembly.
- Improper functioning of a customer baseboard can accidentally delete boot-up code from the CM-T3730, or even damage the module's hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab's SB-T35 baseboard.
- It is recommended to assemble more that one baseboard for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics' Implementation

8.3.1 Magnetics' Selection

Refer to the table below for compatible magnetics. Magnetics listed under the "Qualified" title have been tested in order to verify proper operation with the LAN9220 device. Magnetics in the "Suggested" category have been evaluated on the vendor-supplied datasheet level, but have not been tested. Designers should test and qualify all magnetics before using them in an application.

Table 52 Compatible Magnetics

Vendor	P/N	Package
Qualified Magnetics		
UDE	RTA-1D4B8V1A	Integrated RJ45
Pulse	H1102	16-pin SOIC
Halo	TG110-RP55N5	16-pin SOIC
Halo	HFJ11-RP26E-L12RL	Integrated RJ45
Delta	RJSE1R5310A	Integrated RJ45
Suggested Magnetics		
Pulse	J0011D01B	Integrated RJ45
Bothhand	TS6121C	16-pin SOIC
Bothhand	LU1S041X-43	Integrated RJ45

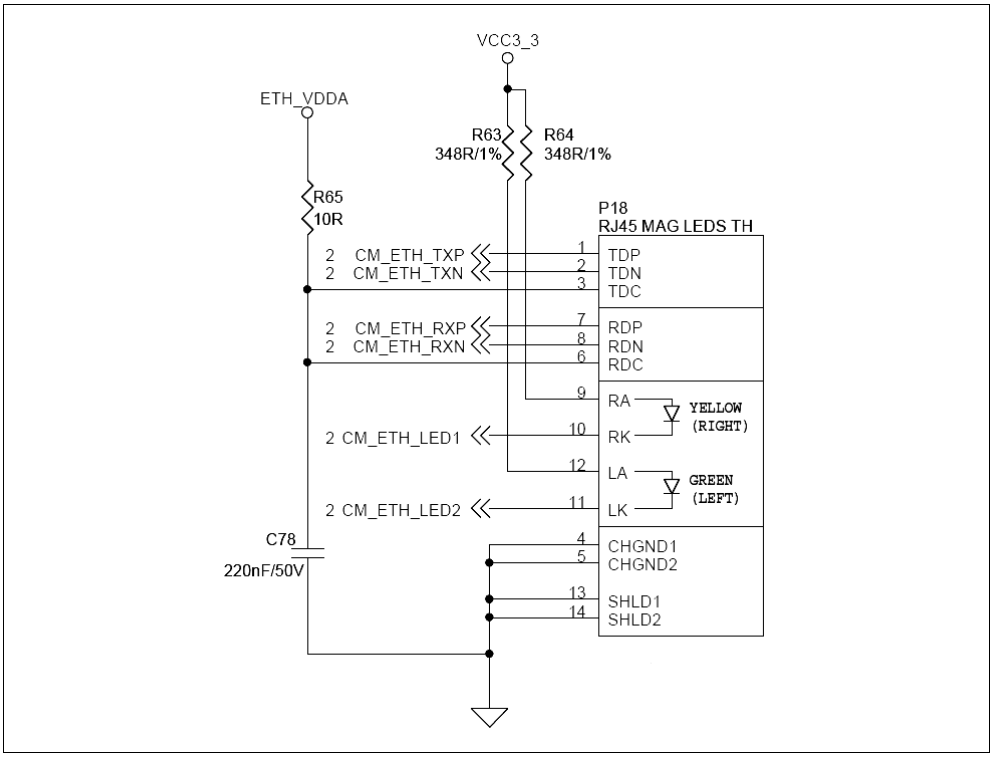
8.3.2 Magnetics' Connection

The center tap connection on the CM-T3730 side for the transmit channel must be connected to a 3.3V analog power rail (can be created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. Decouple the 3.3V voltage with at least one large and one small capacitor (10uF and 0.1uF respectively). The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

The center tap connection on the CM-T3730 side for the receive channel is connected to the transmit channel center tap on the magnetics. In addition, a 0.022 µF capacitor is required from the receive channel center tap of the magnetics to digital ground.

The figure below shows an implementation example with a magnetic embedded in the RJ-45 socket with integrated LED's.

Figure 6 Magnetics' connection example



8.4 Battery Powered Design

The power management sub-system of the CM-T3730 is designed for direct operation with a Li-Ion or a Li-poly battery. Battery charging and supervision functions must be implemented on the baseboard. Please refer to SB-T35 design package for a comprehensive reference design.