MCM-iMX93

Reference Guide

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Table 1 Revision Notes

Date	Description
May 2024	• Initial release
October 2024	• Fixed GND pin numbering in table #54

Please check for a newer revision of this manual at the Compulab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version that you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program Compulab MCM-iMX93 System-on-Module.

1.2 MCM-iMX93 Part Number Legend

Please refer to the Compulab website 'Ordering information' section to decode the MCM-iMX93 part number: https://www.compulab.com/products/computer-on-modules/mcm-imx93-nxp-i-mx-93-som-smd-system-on-module/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
MCM-iMX93 Developer Resources	https://www.compulab.com/products/computer-on-modules/mcm-imx93-nxp-i-mx-93-som-smd-system-on-module/#devres
i.MX93 Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-9-processors/i-mx-93-applications-processor-family-arm-cortex-a55-ml-acceleration-power-efficient-mpu:i.MX93
i.MX93 Datasheet	

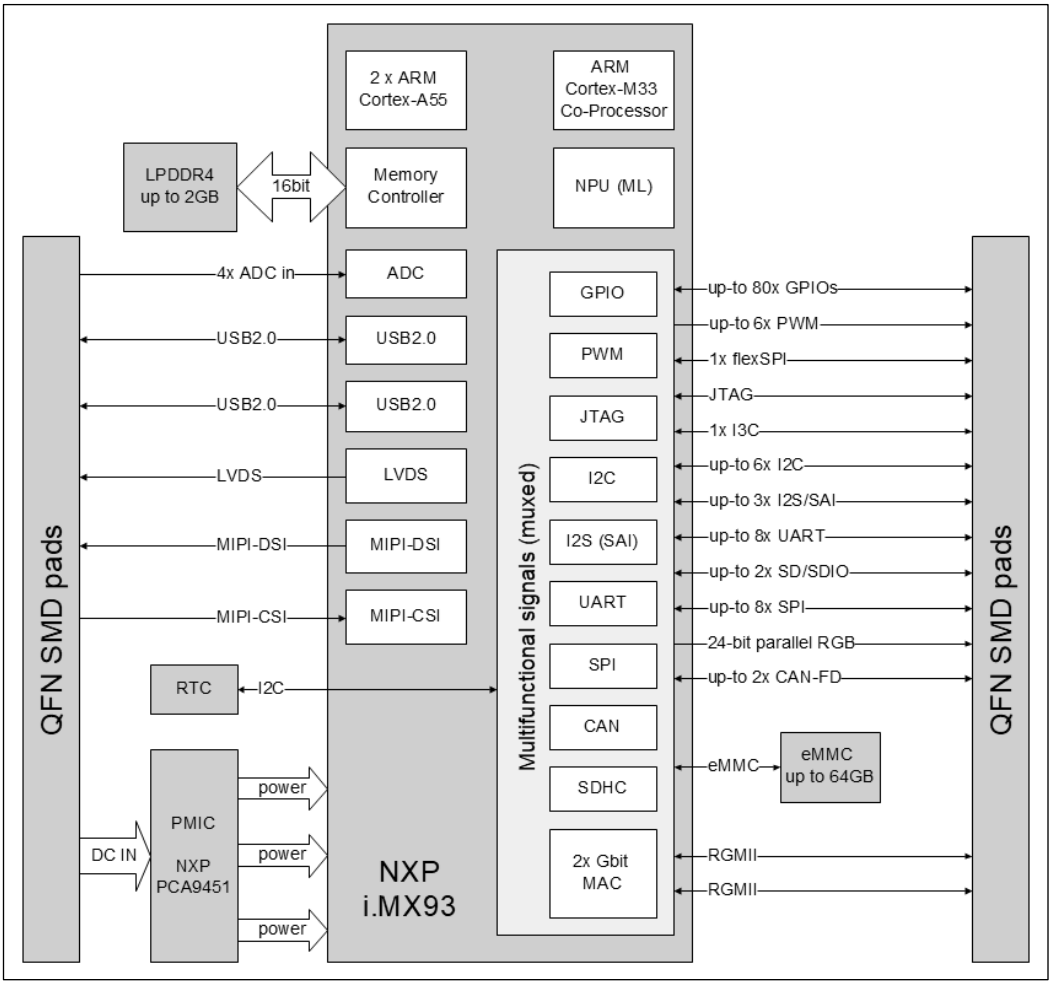
2 OVERVIEW

2.1 Highlights

- NXP i.MX93 / i.MX91 processor, up-to 1.7GHz
- Up to 2GB LPDDR4 and 64GB eMMC
- Integrated AI/ML Neural Processing Unit
- LVDS, MIPI-DSI and MIPI-CSI
- 2x RGMII, 2x USB, 2x CAN-FD, 8x UART
- Tiny size and weight - 30 x 30 x 3 mm, 5 gram

2.2 Block Diagram

Figure 1 MCM-iMX93 Block Diagram



2.3 Specifications

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX9352, dual-core ARM Cortex-A55, 1.7GHz	C1700D
	NXP i.MX9331, single-core ARM Cortex-A55, 1.7GHz	C1700S
NPU	AI/ML Neural Processing Unit Arm® Ethos™ U-65 microNPU	C1700D
Real-Time Co-processor	ARM Cortex-M33, 250Mhz	+
Memory and Storage		
RAM	512MB – 2GB, LPDDR4	D
Storage	eMMC flash, 8GB - 64GB	N
Display, Camera and Audio		
Display	MIPI-DSI, 4 data lanes, up to 1080p60	+
	LVDS, 4 lanes, up to 1366x768 p60	+
	Parallel RGB, 24-bit, up to 1366x768 p60	+
Touchscreen	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	MIPI-CSI, 2 data lanes	+
Audio	Up-to 3x I2S / SAI	+
	S/PDIF input/output	+
Network		
RGMII	2x Ethernet RGMII	+
I/O		
USB	2x USB2.0 dual-role ports	+
UART	Up to 8x UART	+
CAN bus	Up-to 2x CAN-FD	+
SD/SDIO	2x SD/SDIO	+
SPI	Up to 8x SPI	+
I2C	Up to 6x I2C	+
I3C	1x I3C	
ADC	4x general-purpose ADC channels	
PWM	Up to 6x PWM signals	+
GPIO	Up to 80x GPIOs	+
System Logic		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

Electrical Specifications	
Supply Voltage	3.45V to 5.5V

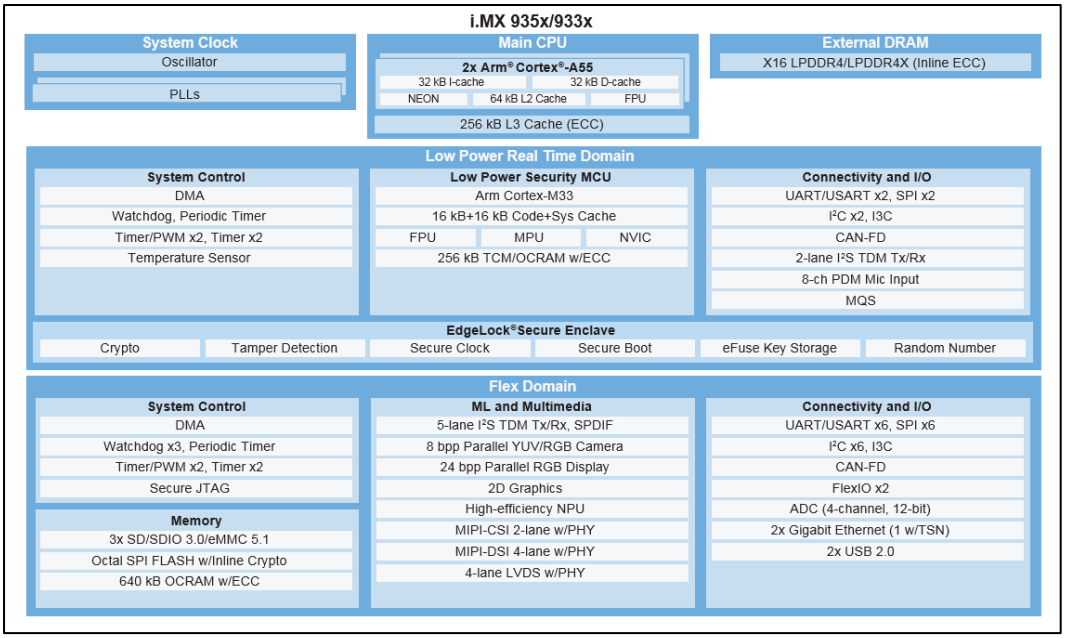
Digital I/O voltage	3.3V / 1.8V
Power consumption	0.5 - 3 W, depending on system load and board configuration
Mechanical Specifications	
Dimensions	30 x 30 x 3 mm
Weight	5 gram
Connectors	140-pin, 0.8mm pitch QFN
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 i.MX93 System-on-Chip

The i.MX 93 System-on-Chip (SoC) includes powerful dual Arm® Cortex®-A55 processors with speeds up to 1.7 GHz integrated with a NPU that accelerates machine learning inference. A general-purpose Arm® Cortex®-M33 running up to 250 MHz is for real-time and low-power processing.

Figure 2 i.MX 93 Block Diagram



3.2 Memory

3.2.1 DRAM

MCM-iMX93 is equipped with up to 2GB of onboard LPDDR4 memory. The LPDDR4 channel is 16-bits wide.

3.2.2 eMMC Storage

MCM-iMX93 uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is intended to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

MCM-iMX93 implements a variety of peripheral interfaces through the 140-pad carrier board footprint. The following notes apply to interfaces available through the carrier-board connectors:

- Some of the MCM-iMX93 carrier board interface pads are multifunctional. Up to 8 functions (ALT modes) are accessible through each multifunctional pad. For additional details, please refer to chapter 5.6.
- MCM-iMX93 uses different I/O voltage domains to power different groups of digital signals. Some signals operate at 3.3V, some at 1.8V. Voltage domain of each signal is specified in the “Signals description” table for each interface.

The signals for each interface are described in the “Signal description” table for the interface in question. The following notes provide information on the “Signal description” tables:

- **“Signal name”** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **“Pin#” –** Pin number on the carrier board interface footprint
- **“Type” –** Signal type, see the definition of different signal types below
- **“Description” –** Signal description with regards to the interface in question
- **“Voltage Domain”** – Voltage level of the particular signal
- **“Availability” –** Depending on MCM-iMX93 configuration options, certain carrier board interface pins are physically disconnected (floating). The “Availability” column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be “available” unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the “Signal description” tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The “Type” column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **“AI”** – Analog Input
- **“AO”** – Analog Output
- **“AIO”** – Analog Input/Output
- **“AP”** – Analog Power Output
- **“I”** – Digital Input
- **"O"** – Digital Output
- **“IO”** – Digital Input/Output
- **“P”** – Power
- **"PD" -** Always pulled down onboard MCM-iMX93, followed by pull value.
- **"PU" -** Always pulled up onboard MCM-iMX93, followed by pull value.
- **“LVDS” -** Low-voltage differential signaling.

4.1 Display Interfaces

4.1.1 MIPI-DSI

The MCM-iMX93 MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX93 SoC. The following main features are supported:

- Compliant with MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2
- Maximum data rate per lane of 1.5 Gbps
- Maximum resolution ranges up to 1920 x 1200 p60

The following table below summarizes the MIPI-DSI interface signals.

Table 5 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description
DSI_CLK_N	24	AO	Negative part of MIPI-DSI clock diff-pair
DSI_CLK_P	25	AO	Positive part of MIPI-DSI clock diff-pair
DSI_D0_N	32	AO	Negative part of MIPI-DSI data diff-pair 0
DSI_D0_P	33	AO	Positive part of MIPI-DSI data diff-pair 0
DSI_D1_N	30	AO	Negative part of MIPI-DSI data diff-pair 1
DSI_D1_P	31	AO	Positive part of MIPI-DSI data diff-pair 1
DSI_D2_N	28	AO	Negative part of MIPI-DSI data diff-pair 2
DSI_D2_P	29	AO	Positive part of MIPI-DSI data diff-pair 2
DSI_D3_N	27	AO	Negative part of MIPI-DSI data diff-pair 3
DSI_D3_P	26	AO	Positive part of MIPI-DSI data diff-pair 3

4.1.2 LVDS Interface

MCM-iMX93 provides one LVDS interface derived from the i.MX93 LVDS display bridge. It supports the following key features:

- Single channel (4 lanes) output at up to 80MHz pixel clock
- Resolutions of up to 1366 x 768 p60 or 1280 x 800 p60

The table below summarizes the LVDS interface signals.

Table 6 LVDS Interface Signals

Signal Name	Pin #	Type	Description
LVDS_CLK_N	38	AO	Negative part of LVDS clock diff-pair
LVDS_CLK_P	39	AO	Positive part of LVDS clock diff-pair
LVDS_D0_N	34	AO	Negative part of LVDS data diff-pair 0
LVDS_D0_P	35	AO	Positive part of LVDS data diff-pair 0
LVDS_D1_N	36	AO	Negative part of LVDS data diff-pair 1
LVDS_D1_P	37	AO	Positive part of LVDS data diff-pair 1
LVDS_D2_N	40	AO	Negative part of LVDS data diff-pair 2
LVDS_D2_P	41	AO	Positive part of LVDS data diff-pair 2
LVDS_D3_N	42	AO	Negative part of LVDS data diff-pair 3
LVDS_D3_P	43	AO	Positive part of LVDS data diff-pair 3

4.1.3 Parallel RGB

MCM-iMX93 provides one parallel RGB interface derived from the i.MX93 LCDIF display module. It supports the following key features:

- 24-bit interface
- Resolutions of up to 1366 x 768 p60 or 1280 x 800 p60

The table below summarizes the parallel RGB interface signals.

Table 7 Parallel RGB Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
LCDIF_PCLK	129	O	Pixel clock used to drive the display panel	3.3V
LCDIF_DE	45	O	Data Enable. Indicates when there is valid pixel data	3.3V
LCDIF_VSYNC	128	O	Vertical Sync signal, indicating the beginning of a new frame	3.3V
LCDIF_HSYNC	108	O	Horizontal Sync signal, indicating the beginning of a new line	3.3V
LCDIF_D[0]	125	O	LCD data output 0	3.3V
LCDIF_D[1]	124	O	LCD data output 1	3.3V
LCDIF_D[2]	107	O	LCD data output 2	3.3V
LCDIF_D[3]	106	O	LCD data output 3	3.3V
LCDIF_D[4]	120	O	LCD data output 4	3.3V
LCDIF_D[5]	121	O	LCD data output 5	3.3V
LCDIF_D[6]	123	O	LCD data output 6	3.3V
LCDIF_D[7]	122	O	LCD data output 7	3.3V
LCDIF_D[8]	105	O	LCD data output 8	3.3V
LCDIF_D[9]	104	O	LCD data output 9	3.3V
LCDIF_D[10]	102	O	LCD data output 10	3.3V
LCDIF_D[11]	103	O	LCD data output 11	3.3V
LCDIF_D[12]	101	O	LCD data output 12	3.3V
LCDIF_D[13]	100	O	LCD data output 13	3.3V
LCDIF_D[14]	118	O	LCD data output 14	3.3V
LCDIF_D[15]	119	O	LCD data output 15	3.3V
LCDIF_D[16]	116	O	LCD data output 16	3.3V
LCDIF_D[17]	117	O	LCD data output 17	3.3V
LCDIF_D[18]	115	O	LCD data output 18	3.3V
LCDIF_D[19]	96	O	LCD data output 19	3.3V
LCDIF_D[20]	99	O	LCD data output 20	3.3V
LCDIF_D[21]	95	O	LCD data output 21	3.3V
LCDIF_D[22]	47	O	LCD data output 22	3.3V
LCDIF_D[23]	48	O	LCD data output 23	3.3V

NOTE: parallel RGB signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.2 Camera Interface

MCM-iMX93 provides one MIPI-CSI interface, derived from the MIPI CSI host controller integrated into the i.MX93 SoC. The controller supports the following main features:

- Up to two data lanes and one clock lane
- Complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2

Please refer to the i.MX93 Reference manual for additional details. The following table summarizes MIPI-CSI signals.

Table 8 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description
CSI_CLK_N	18	AI	Negative part of MIPI-CSI1 clock diff-pair
CSI_CLK_P	19	AI	Positive part of MIPI-CSI1 clock diff-pair
CSI_D0_N	21	AI	Negative part of MIPI-CSI1 data diff-pair 0
CSI_D0_P	20	AI	Positive part of MIPI-CSI1 data diff-pair 0
CSI_D1_N	23	AI	Negative part of MIPI-CSI11 data diff-pair 1
CSI_D1_P	22	AI	Positive part of MIPI-CSI1 data diff-pair 1

4.3 Audio Interfaces

4.3.1 S/PDIF

MCM-iMX93 provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX93 Reference manual for additional details. The following table summarizes the S/PDIF interface signals.

Table 9 S/PDIF Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPDIF_IN	115	I	SPDIF input data line signal	3.3V
	60			1.8V
	62			1.8V
SPDIF_OUT	96	O	SPDIF output data line signal	3.3V
	62			1.8V

NOTE: S/PDIF signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.3.2 SAI

MCM-iMX93 supports up-to three synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

Please refer to the i.MX93 Reference manual for additional details. The tables below summarize the SAI interface signals.

Table 10 SAI1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI1_MCLK	133	IO	Audio master clock. An input when generated externally and an output when generated internally.	3.3V
	131			3.3V
SAI1_RX_DATA[0]	131	I	Receive data, sampled synchronously by the bit clock	3.3V
SAI1_TX_DATA[0]	66	O	Transmit data signal synchronous to bit clock.	3.3V
SAI1_TX_DATA[1]	126*	O	Transmit data signal synchronous to bit clock.	3.3V
SAI1_TX_BCLK	132	O	Transmit bit clock. An input when generated externally and an output when generated internally.	3.3V
SAI1_TX_SYNC	126*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	3.3V

NOTE: SAI1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pads denoted with "*" act as SoC boot-straps and must not be driven during SOM power-up and reset.

Table 11 SAI2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI2_MCLK	61	IO	Audio master clock. An input when generated externally and an output when generated internally.	1.8V
SAI2_RX_DATA[0]	51	I	Receive data, sampled synchronously by the bit clock	1.8V
SAI2_RX_DATA[1]	55	I	Receive data, sampled synchronously by the bit clock	1.8V
SAI2_RX_DATA[2]	53	I	Receive data, sampled synchronously by the bit clock	1.8V
SAI2_RX_DATA[3]	52	I	Receive data, sampled synchronously by the bit clock	1.8V
SAI2_RX_BCLK	49	I	Receive bit clock. An input when generated externally and an output when generated internally.	1.8V
SAI2_RX_SYNC	50	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	1.8V
SAI2_TX_DATA[0]	58	O	Transmit data signal synchronous to bit clock.	1.8V
SAI2_TX_DATA[1]	57	O	Transmit data signal synchronous to bit clock.	1.8V

Signal Name	Pin #	Type	Description	Voltage Domain
SAI2_TX_DATA[2]	59	O	Transmit data signal synchronous to bit clock.	1.8V
SAI2_TX_DATA[3]	60	O	Transmit data signal synchronous to bit clock.	1.8V
SAI2_TX_BCLK	56	O	Transmit bit clock. An input when generated externally and an output when generated internally.	1.8V
SAI2_TX_SYNC	54	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	1.8V

NOTE: SAI2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 12 SAI3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI3_MCLK	100	IO	Audio master clock. An input when generated externally and an output when generated internally.	3.3V
SAI3_RX_DATA[0]	116	I	Receive data, sampled synchronously by the bit clock	3.3V
SAI3_RX_BCLK	118	I	Receive bit clock. An input when generated externally and an output when generated internally.	3.3V
	117			3.3V
SAI3_RX_SYNC	119	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	3.3V
	105			3.3V
SAI3_TX_DATA[0]	117	O	Transmit data signal synchronous to bit clock.	3.3V
	119			3.3V
SAI3_TX_BCLK	101	O	Transmit bit clock. An input when generated externally and an output when generated internally.	3.3V
SAI3_TX_SYNC	47	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	3.3V

NOTE: SAI3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.3.3 MQS

MCM-iMX93 supports two MOQ interfaces that can be used to generate medium quality audio via standard GPIO.

Please refer to the i.MX93 Reference manual for additional details. The following table summarizes the S/PDIF interface signals.

Table 13 MQS Signals

Signal Name	Pin #	Type	Description	Voltage Domain
MQS1_LEFT	126*	O	Left signal output	3.3V
MQS1_RIGHT	131	O	Right signal output	3.3V
MQS2_LEFT	77	O	Left signal output	1.8
	62			1.8
MQS2_RIGHT	80	O	Right signal output	1.8

Signal Name	Pin #	Type	Description	Voltage Domain
	61			1.8

NOTE: MQS signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pads denoted with "*" act as SoC boot-straps and must not be driven during SOM power-up and reset.

4.4 RGMII

MCM-iMX93 features two RMGII interfaces.

The tables below summarize the Ethernet RGMII interface signals.

Table 14 RGMII ENET1 (QOS) Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ENET1_MDC	94	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	1.8V
ENET1_MDIO	93	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	1.8V 1.8V
ENET1_RD0	88	I	Ethernet input data from the PHY	1.8V
ENET1_RD1	90	I	Ethernet input data from the PHY	1.8V
ENET1_RD2	91	I	Ethernet input data from the PHY	1.8V
ENET1_RD3	92	I	Ethernet input data from the PHY	1.8V
ENET1_RX_CTL	87	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	1.8V
ENET1_RXC	89	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	1.8V
ENET1_TD0	84	O	Ethernet output data to PHY	1.8V
ENET1_TD1	82	O	Ethernet output data to PHY	1.8V
ENET1_TD2	83	O	Ethernet output data to PHY	1.8V
ENET1_TD3	85	O	Ethernet output data to PHY	1.8V
ENET1_TXC	86	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	1.8V
ENET1_TX_CTL	81	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	1.8V
ENET1_1588_ EVENT0_IN	74	I	1588 event input	3.3V/1.8V
ENET1_1588_ EVENT0_OUT	70	O	1588 event output	3.3V/1.8V

NOTE: RGMII ENET1 interface operates at 1.8V voltage level.

NOTE: ENET1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 15 RGMII ENET2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ENET2_MDC	50	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	1.8V
ENET2_MDIO	49	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	1.8V
ENET2_RD0	59	I	Ethernet input data from the PHY	1.8V
ENET2_RD1	60	I	Ethernet input data from the PHY	1.8V
ENET2_RD2	61	I	Ethernet input data from the PHY	1.8V
ENET2_RD3	62	I	Ethernet input data from the PHY	1.8V
ENET2_RX_CTL	58	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	1.8V
ENET2_RXC	57	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	1.8V
ENET2_TD0	52	O	Ethernet output data to PHY	1.8V
ENET2_TD1	53	O	Ethernet output data to PHY	1.8V
ENET2_TD2	55	O	Ethernet output data to PHY	1.8V
ENET2_TD3	51	O	Ethernet output data to PHY	1.8V
ENET2_TXC	56	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	1.8V
ENET2_TX_CTL	54	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	1.8V
ENET2_1588_ EVENT0_IN	73	I	1588 event input	3.3V/1.8V
ENET2_1588_ EVENT0_OUT	72	O	1588 event output	3.3V/1.8V
ENET2_1588_ EVENT1_OUT	68	O	1588 event output	3.3V/1.8V

NOTE: RGMII ENET2 signals operate at 1.8V voltage level.

NOTE: ENET2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.5 USB

MCM-iMX93 provides two dual-role USB2.0 ports. USB port #1 can be configured as host or device, while the second port is configured permanently for host mode.

Please refer to the i.MX93 Reference manual for additional details.

The tables below summarize the USB interface signals.

Table 16 USB port #1 Signals

Signal Name	Pin #	Type	Description
USB1_DN	140	IO	USB2.0 negative data
USB1_DP	139	IO	USB2.0 positive data
USB1_VBUS_DET	2	I	USB1 VBUS detect
USB1_ID	1	I	USB1 ID

Table 17 USB port #2 Signals

Signal Name	Pin #	Type	Description
USB2_DN	137	IO	USB2.0 negative data
USB2_DP	136	IO	USB2.0 positive data
USB2_VBUS_DET	138	I	USB2 VBUS detect
USB2_ID	135	I	USB2 ID

4.6 MMC / SD /SDIO

MCM-iMX93 features two SD/SDIO ports. These ports are derived from the i.MX93 uSDHC2 and uSDHC3 controllers. uSDHC IP supports the following main features:

- Fully compliant with MMC 5.1 command/response sets and physical layer
- Fully compliant with SD 3.0 command/response sets and physical layer

Please refer to the i.MX93 Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals.

Table 18 SD2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SD2_CLK	70	O	Clock for MMC/SD/SDIO card	3.3V/1.8V
SD2_CMD	69	IO	CMD line connect to card	3.3V/1.8V
SD2_DATA0	72	IO	DATA0 line in all modes. Also used to detect busy state	3.3V/1.8V
SD2_DATA1	73	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	3.3V/1.8V
SD2_DATA2	68	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	3.3V/1.8V
SD2_DATA3	67	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	3.3V/1.8V
SD2_RESET_B	65	O	Card hardware reset signal, active LOW	3.3V/1.8V
SD2_CD_B	74	I	Card detection pin	3.3V/1.8V

NOTE: SD2 pins can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSELECT.

NOTE: SD2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 19 SD3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SD3_CLK	109	O	Clock for MMC/SD/SDIO card	1.8V
	115			3.3V
SD3_CMD	113	IO	CMD line connect to card	1.8V
	96			3.3V
SD3_DATA0	114	IO	DATA0 line in all modes. Also used to detect busy state	1.8V
	99			3.3V
SD3_DATA1	112	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	1.8V
	95			3.3V
SD3_DATA2	110	IO		1.8V

Signal Name	Pin #	Type	Description	Voltage Domain
	47		DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	3.3V
SD3_DATA3	111	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	1.8V
	48			3.3V

NOTE: SD3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.7 FlexSPI

MCM-iMX93 provides one FlexSPI port that can support 4-bit serial flash memory or serial RAM devices. Please refer to the i.MX93 Reference manual for additional details.

The following table summarizes the FlexSPI interface signals.

Table 20 FlexSPI Signals

Signal Name	Pin #	Type	Description	Voltage Domain
FLEXSPI_SCLK	109	O	Flash serial clock	1.8V
FLEXSPI_SS0	113	O	Flash chip select	1.8V
FLEXSPI_DATA[0]	114	IO	Flash data 0	1.8V
FLEXSPI_DATA[1]	112	IO	Flash data 1	1.8V
FLEXSPI_DATA[2]	110	IO	Flash data 2	1.8V
FLEXSPI_DATA[3]	111	IO	Flash data 3	1.8V

NOTE: FlexSPI signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.8 UART

MCM-iMX93 features up-to eight UART ports. The i.MX93 UART supports the following features:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 5 Mbps.
- Hardware flow control support for a request to send and clear to send signals.

NOTE: By default UART1 is assigned to be used as the main system console port.

NOTE: By default UART2 is assigned to be used as the M7 core debug port.

Please refer to the i.MX93 Reference manual for additional details.

The tables below summarize the UART interface signals.

Table 21 UART1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART1_CTS	133	I	Clear to send	3.3V
UART1_RTS	130*	O	Request to send	3.3V
UART1_DTR	66*	I	Data terminal ready	3.3V
UART1_DSR	132	O	Data set ready	3.3V
UART1_RXD	64	I	Serial data receive	3.3V
UART1_TXD	63*	O	Serial data transmit	3.3V

NOTE: UART1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pads denoted with "*" act as SoC boot-straps and must not be driven during SOM power-up and reset.

Table 22 UART2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART2_CTS	132	I	Clear to send	3.3V
UART2_RTS	66*	O	Request to send	3.3V
UART2_DSR	131	O	Data set ready	3.3V
UART2_DTR	126*	I	Data terminal ready	3.3V
UART2_RXD	133	I	Serial data receive	3.3V
UART2_TXD	130	O	Serial data transmit	3.3V

NOTE: UART2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pads denoted with "*" act as SoC boot-straps and must not be driven during SOM power-up and reset.

Table 23 UART3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART3_CTS	101	I	Clear to send	3.3V
	90			1.8V
UART3_RTS	100	O	Request to send	3.3V
	82			1.8V
UART3_RXD	103	I	Serial data receive	3.3V
	88			1.8V
UART3_TXD	102	O	Serial data transmit	3.3V
	84			1.8V

NOTE: UART3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 24 UART4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART4_RXD	103	I	Serial data receive	3.3V
	59			1.8V
UART4_TXD	102	O	Serial data transmit	3.3V
	52			1.8V
UART4_CTS	101	I	Clear to send	3.3V
	61			1.8V
UART4_RTS	100	O	Request to send	3.3V
	53			1.8V
UART4_DTR	54	I	Data terminal ready	1.8V
UART4_DSR	58	O	Data set ready	1.8V
UART4_RIN	49	I	Ring indicator	1.8V

NOTE: UART4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 25 UART5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART5_RXD	45	I	UART-5 serial data receive	3.3V
	77			1.8V
UART5_TXD	129	O	UART-5 serial data transmit	3.3V
	80			1.8V
UART5_CTS	128	I	UART-5 clear to send	3.3V
	79			1.8V
UART5_RTS	108	O	UART-5 request to send	3.3V
	78			1.8V

NOTE: UART5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 26 UART6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART6_RXD	124	I	Serial data receive	3.3V
UART6_TXD	125	O	Serial data transmit	3.3V
UART6_CTS	107	I	Clear to send	3.3V
UART6_RTS	106	O	Request to send	3.3V

NOTE: UART6 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 27 UART7 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART7_RXD	121	I	Serial data receive	3.3V
UART7_TXD	120	O	Serial data transmit	3.3V
UART7_CTS	123	I	Clear to send	3.3V
UART7_RTS	122	O	Request to send	3.3V

NOTE: UART7 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 28 UART8 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART8_RXD	104	I	Serial data receive	3.3V
UART8_TXD	105	O	Serial data transmit	3.3V
UART8_CTS	102	I	Clear to send	3.3V
UART8_RTS	103	O	Request to send	3.3V

NOTE: UART8 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.9 CAN-FD

MCM-iMX93 features up-to two CAN-FD interfaces. These interfaces support the following key features:

- Full implementation of the CAN FD protocol and CAN protocol specification version 2.0B
- Compliant with the ISO 11898-1 standard

Please refer to the i.MX93 Reference manual for additional details.

The tables below summarize the CAN interface signals.

Table 29 CAN1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN1_TX	66*	O	CAN transmit pin	3.3V
CAN1_RX	132	I	CAN receive pin	3.3V

Table 30 CAN2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN2_TX	95	O	CAN transmit pin	3.3V
	77			1.8V
	85			1.8V
	72			3.3V/1.8V
CAN2_RX	48	I	CAN receive pin	3.3V
	80			1.8V
	83			1.8V
	73			3.3V/1.8V

NOTE: CAN signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pins denoted “3.3V/1.8V” can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSELECT.

NOTE: Pads denoted with “*” act as SoC boot-straps and must not be driven during SOM power-up and reset.

4.10 SPI

Up-to eight SPI interfaces are accessible through the MCM-iMX93 carrier board interface. The SPI interfaces are derived from i.MX93 integrated low-power SPI modules. The following key features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- One Chip Select (SS) signal
- Direct Memory Access (DMA) support

Please refer to the i.MX93 Reference manual for additional details.

SPI1 and SPI2 channels are limited to maximum frequency of 10MHz.

The following tables summarize the SPI interface signals.

Table 31 SPI1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI1_SIN	132	I	Serial data input	3.3V
SPI1_SOUT	131	O	Master data out; slave data in	3.3V
SPI1_SCLK	66*	O	Master clock out; slave clock in	3.3V
SPI1_PCS0	126*	O	Chip select 0	3.3V

Table 32 SPI2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI2_SIN	64	I	Master data in; slave data out	3.3V
SPI2_SOUT	133	O	Master data out; slave data in	3.3V
SPI2_SCLK	130*	O	Master clock out; slave clock in	3.3V
SPI2_PCS0	63*	O	Chip select 0	3.3V

Table 33 SPI3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI3_SIN	121	I	Master data in; slave data out	3.3V
SPI3_SOUT	123	O	Master data out; slave data in	3.3V
SPI3_SCLK	122	O	Master clock out; slave clock in	3.3V
SPI3_PCS0	120	O	Chip select 0	3.3V
SPI3_PCS1	106	O	Chip select 1	3.3V

NOTE: SPI signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pads denoted with "*" act as SoC boot-straps and must not be driven during SOM power-up and reset.

Table 34 SPI4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI4_SIN	119	I	Master data in; slave data out	3.3V
SPI4_SOUT	116	O	Master data out; slave data in	3.3V
SPI4_SCLK	117	O	Master clock out; slave clock in	3.3V
SPI4_PCS0	118	O	Chip select 0	3.3V
SPI4_PCS1	100	O	Chip select 1	3.3V
SPI4_PCS2	101	O	Chip select 2	3.3V

Table 35 SPI5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI5_SIN	119	I	Master data in; slave data out	3.3V
SPI5_SOUT	116	O	Master data out; slave data in	3.3V
SPI5_SCLK	117	O	Master clock out; slave clock in	3.3V
SPI5_PCS0	118	O	Chip select 0	3.3V
SPI5_PCS1	48	O	Chip select 1	3.3V

Table 36 SPI6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI6_SIN	45	I	Master data in; slave data out	3.3V
SPI6_SOUT	128	O	Master data out; slave data in	3.3V
SPI6_SCLK	108	O	Master clock out; slave clock in	3.3V
SPI6_PCS0	129	O	Chip select 0	3.3V

Table 37 SPI7 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI7_SIN	124	I	Master data in; slave data out	3.3V
SPI7_SOUT	107	O	Master data out; slave data in	3.3V
SPI7_SCLK	106	O	Master clock out; slave clock in	3.3V
SPI7_PCS0	125	O	Chip select 0	3.3V
SPI7_PCS1	95	O	Chip select 1	3.3V

NOTE: SPI signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 38 SPI8 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI8_SIN	104	I	Master data in; slave data out	3.3V
SPI8_SOUT	102	O	Master data out; slave data in	3.3V
SPI8_SCLK	103	O	Master clock out; slave clock in	3.3V
SPI8_PCS0	105	O	Chip select 0	3.3V
SPI8_PCS1	47	O	Chip select 1	3.3V

NOTE: SPI signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.11 I2C

MCM-iMX93 features up-to six I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)

Please refer to the i.MX93 Reference manual for additional details.

The tables below summarize the I2C interface signals.

Table 39 I2C3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C3_SCL	45	O	I2C serial clock line	3.3V
	97			3.3V
I2C3_SDA	129	IO	I2C serial data line	3.3V
	98			3.3V

Table 40 I2C4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C4_SCL	108	O	I2C serial clock line	3.3V
I2C4_SDA	128	IO	I2C serial data line	3.3V

Table 41 I2C5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C5_SCL	45	O	I2C serial clock line	3.3V
	96			3.3V
I2C5_SDA	129	IO	I2C serial data line	3.3V
	115			3.3V

NOTE: I2C signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 42 I2C6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C6_SCL	108	O	I2C serial clock line	3.3V
	124			3.3V
I2C6_SDA	128	IO	I2C serial data line	3.3V
	125			3.3V

Table 43 I2C7 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C7_SCL	121	O	I2C serial clock line	3.3V
	106			3.3V
I2C7_SDA	120	IO	I2C serial data line	3.3V
	107			3.3V

Table 44 I2C8 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C8_SCL	104	O	I2C serial clock line	3.3V
	122			3.3V
I2C8_SDA	123	IO	I2C serial data line	3.3V
	105			3.3V

NOTE: I2C signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.12 I3C

MCM-iMX93 supports one I3C bus interface. Please refer to the i.MX93 Reference manual for additional details. The tables below summarize the I3C interface signals.

Table 45 I3C2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I3C2_SCL	74	O	Serial clock line	3.3V/1.8V
	94			1.8V
I3C2_SDA	70	IO	Serial data line	3.3V/1.8V
	93			1.8V
I3C2_PUR	69	O	Pull up resistance. There is internal pull-up resistance on SDA, which is controlled by the I3C controller. If the internal pullup is not enough, PUR can be used to control an external pull-up resistance on SDA actively.	3.3V/1.8V
	82			1.8V

NOTE: I3C signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pins denoted "3.3V/1.8V" can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSELECT.

4.13 Timer/Pulse Width Modulation

i.MX93 supports multi-channel timer modules (TPM) that can be used for electric motor control and power management. Please refer to the i.MX93 Reference manual for additional details.

The tables below summarize the PDM interface signals.

Table 46 TPM1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
TPM1_CH0	64	IO	Channel 0 I/O pin	3.3V
TPM1_CH1	63*	IO	Channel 1 I/O pin	3.3V
TPM1_CH2	133	IO	Channel 2 I/O pin	3.3V
TPM1_CH3	130*	IO	Channel 3 I/O pin	3.3V

NOTE: Pads denoted with "*" act as SoC boot-straps and must not be driven during SOM power-up and reset.

Table 47 TPM3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
TPM3_EXTCLK	121	I	External clock	3.3V
TPM3_CH0	125	IO	Channel 0 I/O pin	3.3V
TPM3_CH1	116	IO	Channel 1 I/O pin	3.3V
TPM3_CH2	105	IO	Channel 2 I/O pin	3.3V
TPM3_CH3	99	IO	Channel 3 I/O pin	3.3V

Table 48 TPM4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
TPM4_EXTCLK	123	I	External clock	3.3V
TPM4_CH0	124	IO	Channel 0 I/O pin	3.3V
TPM4_CH1	117	IO	Channel 1 I/O pin	3.3V
TPM4_CH2	104	IO	Channel 2 I/O pin	3.3V
TPM4_CH3	95	IO	Channel 3 I/O pin	3.3V

Table 49 TPM5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
TPM5_EXTCLK	122	I	External clock	3.3V
TPM5_CH0	107	IO	Channel 0 I/O pin	3.3V
TPM5_CH1	115	IO	Channel 1 I/O pin	3.3V
TPM5_CH2	118	IO	Channel 2 I/O pin	3.3V

NOTE: TPM signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.14 ADC

MCM-iMX93 features a 4-channel 12-bit ADC implemented in the i.MX93 SoC.

Please refer to the i.MX93 Reference manual for additional details.

The following table summarizes ADC signals.

Table 50 ADC Signals

Signal Name	Pin #	Type	Description
ADC_IN0	10	AI	ADC input channel 0
ADC_IN1	9	AI	ADC input channel 1
ADC_IN2	8	AI	ADC input channel 2
ADC_IN3	7	AI	ADC input channel 3

4.15 Tamper

i.MX93 supports two tamper pins – two passive or one active.

For additional details please refer to the i.MX93 Security Reference manual.

The following table summarizes tamper signals.

Table 51 Tamper Signals

Signal Name	Pin #	Type	Description
TAMPER0	12	IO	Tamper channel 0
TAMPER1	13	IO	Tamper channel 1

4.16 JTAG

MCM-iMX93 enables access to the i.MX93 JTAG port through the carrier board interface.

Please refer to the i.MX93 Reference manual for additional details.

The table below summarizes the JTAG interface signals.

Table 52 JTAG Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
JTAG_TCK	79	I	Test clock	1.8V
JTAG_TDI	77	I	Test data in	1.8V
JTAG_TDO	80	O	Test data out	1.8V
JTAG_TMS	78	I	Test mode select	1.8V

NOTE: JTAG interface operates at 1.8V voltage level.

4.17 GPIO

Up-to 80 of the i.MX93 general purpose input/output (GPIO) signals are available through the MCM-iMX93 carrier board interface. In addition, GPIO signals can produce interrupts.

Please refer to the i.MX93 Reference manual for additional details. The following table summarizes the GPIO interface signals.

Table 53 GPIO Signals

Signal Name	Pin #	Type	Description	Voltage Domain
GPIO1_IO[4]	64	IO	General-purpose input/output	3.3V
GPIO1_IO[6]	133	IO	General-purpose input/output	3.3V
GPIO1_IO[12]	132	IO	General-purpose input/output	3.3V
GPIO1_IO[14]	131	IO	General-purpose input/output	3.3V
GPIO2_IO[0]	129	IO	General-purpose input/output	3.3V
GPIO2_IO[1]	45	IO	General-purpose input/output	3.3V
GPIO2_IO[2]	128	IO	General-purpose input/output	3.3V
GPIO2_IO[3]	108	IO	General-purpose input/output	3.3V
GPIO2_IO[4]	125	IO	General-purpose input/output	3.3V
GPIO2_IO[5]	124	IO	General-purpose input/output	3.3V
GPIO2_IO[6]	107	IO	General-purpose input/output	3.3V
GPIO2_IO[7]	106	IO	General-purpose input/output	3.3V
GPIO2_IO[8]	120	IO	General-purpose input/output	3.3V
GPIO2_IO[9]	121	IO	General-purpose input/output	3.3V
GPIO2_IO[10]	123	IO	General-purpose input/output	3.3V
GPIO2_IO[11]	122	IO	General-purpose input/output	3.3V
GPIO2_IO[12]	105	IO	General-purpose input/output	3.3V
GPIO2_IO[13]	104	IO	General-purpose input/output	3.3V
GPIO2_IO[14]	102	IO	General-purpose input/output	3.3V
GPIO2_IO[15]	103	IO	General-purpose input/output	3.3V
GPIO2_IO[16]	101	IO	General-purpose input/output	3.3V
GPIO2_IO[17]	100	IO	General-purpose input/output	3.3V
GPIO2_IO[18]	118	IO	General-purpose input/output	3.3V
GPIO2_IO[19]	119	IO	General-purpose input/output	3.3V
GPIO2_IO[20]	116	IO	General-purpose input/output	3.3V
GPIO2_IO[21]	117	IO	General-purpose input/output	3.3V
GPIO2_IO[22]	115	IO	General-purpose input/output	3.3V
GPIO2_IO[23]	96	IO	General-purpose input/output	3.3V
GPIO2_IO[24]	99	IO	General-purpose input/output	3.3V
GPIO2_IO[25]	95	IO	General-purpose input/output	3.3V
GPIO2_IO[26]	47	IO	General-purpose input/output	3.3V
GPIO2_IO[27]	48	IO	General-purpose input/output	3.3V
GPIO2_IO[28]	98	IO	General-purpose input/output	3.3V
GPIO2_IO[29]	97	IO	General-purpose input/output	3.3V
GPIO3_IO[0]	74	IO	General-purpose input/output	3.3V / 1.8V
GPIO3_IO[1]	70	IO	General-purpose input/output	3.3V / 1.8V
GPIO3_IO[2]	69	IO	General-purpose input/output	3.3V / 1.8V
GPIO3_IO[3]	72	IO	General-purpose input/output	3.3V / 1.8V
GPIO3_IO[4]	73	IO	General-purpose input/output	3.3V / 1.8V

GPIO3_IO[5]	68	IO	General-purpose input/output	3.3V / 1.8V
GPIO3_IO[6]	67	IO	General-purpose input/output	3.3V / 1.8V
GPIO3_IO[7]	65	IO	General-purpose input/output	3.3V / 1.8V
GPIO3_IO[20]	109	IO	General-purpose input/output	1.8V
GPIO3_IO[21]	113	IO	General-purpose input/output	1.8V
GPIO3_IO[22]	114	IO	General-purpose input/output	1.8V
GPIO3_IO[23]	112	IO	General-purpose input/output	1.8V
GPIO3_IO[24]	110	IO	General-purpose input/output	1.8V
GPIO3_IO[25]	111	IO	General-purpose input/output	1.8V
GPIO3_IO[28]	77	IO	General-purpose input/output	1.8V
GPIO3_IO[29]	78	IO	General-purpose input/output	1.8V
GPIO3_IO[30]	79	IO	General-purpose input/output	1.8V
GPIO3_IO[31]	80	IO	General-purpose input/output	1.8V
GPIO4_IO[0]	94	IO	General-purpose input/output	1.8V
GPIO4_IO[1]	93	IO	General-purpose input/output	1.8V
GPIO4_IO[2]	85	IO	General-purpose input/output	1.8V
GPIO4_IO[3]	83	IO	General-purpose input/output	1.8V
GPIO4_IO[4]	82	IO	General-purpose input/output	1.8V
GPIO4_IO[5]	84	IO	General-purpose input/output	1.8V
GPIO4_IO[6]	81	IO	General-purpose input/output	1.8V
GPIO4_IO[7]	86	IO	General-purpose input/output	1.8V
GPIO4_IO[8]	87	IO	General-purpose input/output	1.8V
GPIO4_IO[9]	89	IO	General-purpose input/output	1.8V
GPIO4_IO[10]	88	IO	General-purpose input/output	1.8V
GPIO4_IO[11]	90	IO	General-purpose input/output	1.8V
GPIO4_IO[12]	91	IO	General-purpose input/output	1.8V
GPIO4_IO[13]	92	IO	General-purpose input/output	1.8V
GPIO4_IO[14]	50	IO	General-purpose input/output	1.8V
GPIO4_IO[15]	49	IO	General-purpose input/output	1.8V
GPIO4_IO[16]	51	IO	General-purpose input/output	1.8V
GPIO4_IO[17]	55	IO	General-purpose input/output	1.8V
GPIO4_IO[18]	53	IO	General-purpose input/output	1.8V
GPIO4_IO[19]	52	IO	General-purpose input/output	1.8V
GPIO4_IO[20]	54	IO	General-purpose input/output	1.8V
GPIO4_IO[21]	56	IO	General-purpose input/output	1.8V
GPIO4_IO[22]	58	IO	General-purpose input/output	1.8V
GPIO4_IO[23]	57	IO	General-purpose input/output	1.8V
GPIO4_IO[24]	59	IO	General-purpose input/output	1.8V
GPIO4_IO[25]	60	IO	General-purpose input/output	1.8V
GPIO4_IO[26]	61	IO	General-purpose input/output	1.8V
GPIO4_IO[27]	62	IO	General-purpose input/output	1.8V

NOTE: GPIO signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pins denoted “3.3V/1.8V” can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSELECT.

5 SYSTEM LOGIC

5.1 Power Supply

Table 54 Power signals

Signal Name	Pin#	Type	Description
V_SOM	4, 6, 11, 15	P	Main power supply. Connect to a regulated DC supply or Li-Ion battery
VCC_RTC	127	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. If RTC back-up is not required, connect this pin to GND.
VSD_3V3	134	PO	3.3V regulator output. Should be used to supply power to SD card connected to SD2 interface
GND	75 G1, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17, G18, G19, G20, G21, G22, G23, G24, G25, G26, G27, G28	P	Common ground

5.2 I/O Voltage Domains

MCM-iMX93 utilizes three separate I/O voltage domains that are used to power different I/O modules of the i.MX93 SoC. Some pins operate at 3.3V, some at 1.8V.

Voltage domain of each signal is specified in the peripheral interface signals tables.

NOTE: Carrier-board designer must ensure that voltage level of the I/O pins matches the I/O voltage of the peripheral ICs on the carrier-board.

5.3 System and Miscellaneous Signals

5.3.1 Power management

MCM-iMX93 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX93 SoC. The logic that controls both signals is supplied by the i.MX93 SoC SNVS power rail.

The PMIC_STBY_REQ output can be used to signal the carrier board power supply that MCM-iMX93 is in ‘standby’ or ‘OFF’ mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX93 Reference manual for additional details. The table below summarizes the external regulator control signals.

Table 55 External regulator control signals

Signal Name	Pin #	Type	Description
PMIC_STBY_REQ	16	O	When the processor enters SUSPEND mode, it will assert this signal.
PMIC_ON_REQ	44	O	Active high power-up request output from i.MX93 SoC.
ONOFF	3	I	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).

5.4 Reset

SYS_RST_PMIC signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on MCM-iMX93. Please refer to the i.MX93 Reference manual for additional details.

Table 56 Reset signals

Signal Name	Pin #	Type	Description
SYS_RST_PMIC	14	I	Active Low cold reset input signal. Should be used as main system reset
POR_B	46	I	CPU power on reset input pin, active low

5.5 Boot Sequence

MCM-iMX93 boot sequence defines which interface/media is used by MCM-iMX93 to load and execute the initial software (such as SPL or/and U-boot). MCM-iMX93 can load initial software from the following interfaces/media:

- On-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD card using the SD2 interface
- Serial Download boot using USB1 interface

MCM-iMX93 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of three different boot sequences are supported by MCM-iMX93:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternative sequence: designed to allow recovery from an external bootable SD card in case of data corruption of the on-board primary boot device. Using the alternate sequence allows MCM-iMX93 to boot bypassing the onboard eMMC.
- Serial download mode: provides a means to download a program image to the i.MX93 system-on-chip over USB serial connection

Logic values of boot selections signals define which of the supported boot sequences is used by the system.

Table 57 Boot selection signals

Signal Name	Pin #	Type	Description
ALT_BOOT_SD	76	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence
ALT_BOOT_USB	5	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence

Table 58 MCM-iMX93 boot sequences

Mode	ALT_BOOT_SD	ALT_BOOT_USB	Booting sequence
Standard	Low or floating	Low or floating	On-board eMMC (primary boot storage)
Alternative	High	Low or floating	SD card on SD/SDIO2 interface
SDP mode	Low or floating	High	Serial download mode

5.6 Signal Multiplexing Characteristics

Up to 84 of the MCM-iMX93 carrier board interface pads are multifunctional. Multifunctional pins enable extensive functional flexibility of the MCM-iMX93 SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 6 functions (MUX modes) are accessible through each multifunctional carrier board interface pad. The multifunctional capabilities of MCM-iMX93 pads are derived from the i.MX93 SoC control module.

NOTE: Pad function selection is controlled by software.

NOTE: Each pad can be used for a single function at a time.

NOTE: Only one pad can be used for each function (in case a function is available on more than one carrier board interface pad).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 59 Multifunctional Signals

Pad #	SoC Pin Name	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	Voltage Domain
79	**JTAG_TCLK_SWCLK**	JTAG_TCLK_SWCLK					GPIO3_IO[30]	UART5_CTS_B		1.8V
77	**JTAG_TDI**	JTAG_TDI	MQS2_LEFT		CAN2_TX		GPIO3_IO[28]	UART5_RX		1.8V
80	**JTAG_TDO_TRACESWO**	JTAG_TDO	MQS2_RIGHT		CAN2_RX		GPIO3_IO[31]	UART5_TX		1.8V
78	**JTAG_TMS_SWDIO**	JTAG_TMS_SWDIO					GPIO3_IO[29]	UART5_RTS_B		1.8V
94	**ENET1_MDC**	ENET1_MDC	UART3_DCB_B	I3C2_SCL	USB1_OTG_ID		GPIO4_IO[0]			1.8V
93	**ENET1_MDIO**	ENET1_MDIO	UART3_RIN_B	I3C2_SDA	USB1_OTG_PWR		GPIO4_IO[1]			1.8V
88	**ENET1_RD0**	ENET1_RD0	UART3_RX				GPIO4_IO[10]			1.8V
90	**ENET1_RD1**	ENET1_RD1	UART3_CTS_B		LPTMR2_ALT1		GPIO4_IO[11]			1.8V
91	**ENET1_RD2**	ENET1_RD2			LPTMR2_ALT2		GPIO4_IO[12]			1.8V
92	**ENET1_RD3**	ENET1_RD3			LPTMR2_ALT3		GPIO4_IO[13]			1.8V

Pad #	SoC Pin Name	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	Voltage Domain
87	**ENET1_RX_CTL**	ENET1_RX_CTL	UART3_DSR_B		USB2_OTG_PWR		GPIO4_IO[8]			1.8V
89	**ENET1_RXC**	ENET1_RXC	ENET_QOS_RX_ER				GPIO4_IO[9]			1.8V
84	**ENET1_TD0**	ENET1_TD0	UART3_TX				GPIO4_IO[5]			1.8V
82	**ENET1_TD1**	ENET1_TD1	UART3_RTS_B	I3C2_PUR	USB1_OTG_OC		GPIO4_IO[4]	I3C2_PUR_B		1.8V
83	**ENET1_TD2**	ENET1_TD2		CAN2_RX	USB2_OTG_OC		GPIO4_IO[3]			1.8V
85	**ENET1_TD3**	ENET1_TD3		CAN2_TX	USB2_OTG_ID		GPIO4_IO[2]			1.8V
81	**ENET1_TX_CTL**	ENET1_TX_CTL	UART3_DTR_B				GPIO4_IO[6]			1.8V
86	**ENET1_TXC**	ENET1_TXC	ENET_QOS_TX_ER				GPIO4_IO[7]			1.8V
50	**ENET2_MDC**	ENET2_MDC	UART4_DCB_B	SAI2_RX_SYNC			GPIO4_IO[14]			1.8V
49	**ENET2_MDIO**	ENET2_MDIO	UART4_RIN_B	SAI2_RX_BCLK			GPIO4_IO[15]			1.8V
59	**ENET2_RD0**	ENET2_RD0	UART4_RX	SAI2_TX_DATA[2]			GPIO4_IO[24]			1.8V
60	**ENET2_RD1**	ENET2_RD1	SPDIF1_IN	SAI2_TX_DATA[3]			GPIO4_IO[25]			1.8V
61	**ENET2_RD2**	ENET2_RD2	UART4_CTS_B	SAI2_MCLK	MQS2_RIGHT		GPIO4_IO[26]			1.8V
62	**ENET2_RD3**	ENET2_RD3	SPDIF1_OUT	SPDIF1_IN	MQS2_LEFT		GPIO4_IO[27]			1.8V
58	**ENET2_RX_CTL**	ENET2_RX_CTL	UART4_DSR_B	SAI2_TX_DATA[0]			GPIO4_IO[22]			1.8V
57	**ENET2_RXC**	ENET2_RXC	ENET2_RX_ER	SAI2_TX_DATA[1]			GPIO4_IO[23]			1.8V
52	**ENET2_TD0**	ENET2_TD0	UART4_TX	SAI2_RX_DATA[3]			GPIO4_IO[19]			1.8V
53	**ENET2_TD1**	ENET2_TD1	UART4_RTS_B	SAI2_RX_DATA[2]			GPIO4_IO[18]			1.8V
55	**ENET2_TD2**	ENET2_TD2		SAI2_RX_DATA[1]			GPIO4_IO[17]			1.8V
51	**ENET2_TD3**	ENET2_TD3		SAI2_RX_DATA[0]			GPIO4_IO[16]			1.8V
54	**ENET2_TX_CTL**	ENET2_TX_CTL	UART4_DTR_B	SAI2_TX_SYNC			GPIO4_IO[20]			1.8V
56	**ENET2_TXC**	ENET2_TXC	ENET2_TX_ER	SAI2_TX_BCLK			GPIO4_IO[21]			1.8V
129	**GPIO_IO00**	GPIO2_IO[0]	I2C3_SDA	ISI_PCLK	LCDIF_PCLK	SPI6_PCS0	UART5_TX	I2C5_SDA		3.3V
45	**GPIO_IO01**	GPIO2_IO[1]	I2C3_SCL	ISI_D[0]	LCDIF_DE	SPI6_SIN	UART5_RX	I2C5_SCL		3.3V
128	**GPIO_IO02**	GPIO2_IO[2]	I2C4_SDA	ISI_FRAME_VALID	LCDIF_VSYNC	SPI6_SOUT	UART5_CTS_B	I2C6_SDA		3.3V
108	**GPIO_IO03**	GPIO2_IO[3]	I2C4_SCL	ISI_LINE_VALID	LCDIF_HSYNC	SPI6_SCK	UART5_RTS_B	I2C6_SCL		3.3V
125	**GPIO_IO04**	GPIO2_IO[4]	TPM3_CH0	PDM_CLK	LCDIF_D[0]	SPI7_PCS0	UART6_TX	I2C6_SDA		3.3V

Pad #	SoC Pin Name	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	Voltage Domain
124	**GPIO_IO05**	GPIO2_IO[5]	TPM4_CH0	PDM_BIT_STREAM[0]	LCDIF_D[1]	SPI7_SIN	UART6_RX	I2C6_SCL		3.3V
107	**GPIO_IO06**	GPIO2_IO[6]	TPM5_CH0	PDM_BIT_STREAM[1]	LCDIF_D[2]	SPI7_SOUT	UART6_CTS_B	I2C7_SDA		3.3V
106	**GPIO_IO07**	GPIO2_IO[7]	SPI3_PCS1	ISI_D[1]	LCDIF_D[3]	SPI7_SCK	UART6_RTS_B	I2C7_SCL		3.3V
120	**GPIO_IO08**	GPIO2_IO[8]	SPI3_PCS0	ISI_D[2]	LCDIF_D[4]	TPM6_CH0	UART7_TX	I2C7_SDA		3.3V
121	**GPIO_IO09**	GPIO2_IO[9]	SPI3_SIN	ISI_D[3]	LCDIF_D[5]	TPM3_EXTCLK	UART7_RX	I2C7_SCL		3.3V
123	**GPIO_IO10**	GPIO2_IO[10]	SPI3_SOUT	ISI_D[4]	LCDIF_D[6]	TPM4_EXTCLK	UART7_CTS_B	I2C8_SDA		3.3V
122	**GPIO_IO11**	GPIO2_IO[11]	SPI3_SCK	ISI_D[5]	LCDIF_D[7]	TPM5_EXTCLK	UART7_RTS_B	I2C8_SCL		3.3V
105	**GPIO_IO12**	GPIO2_IO[12]	TPM3_CH2	PDM_BIT_STREAM[2]	LCDIF_D[8]	SPI8_PCS0	UART8_TX	I2C8_SDA	SAI3_RX_SYNC	3.3V
104	**GPIO_IO13**	GPIO2_IO[13]	TPM4_CH2	PDM_BIT_STREAM[3]	LCDIF_D[9]	SPI8_SIN	UART8_RX	I2C8_SCL		3.3V
102	**GPIO_IO14**	GPIO2_IO[14]	UART3_TX	ISI_D[6]	LCDIF_D[10]	SPI8_SOUT	UART8_CTS_B	UART4_TX		3.3V
103	**GPIO_IO15**	GPIO2_IO[15]	UART3_RX	ISI_D[7]	LCDIF_D[11]	SPI8_SCK	UART8_RTS_B	UART4_RX		3.3V
101	**GPIO_IO16**	GPIO2_IO[16]	SAI3_TX_BCLK	PDM_BIT_STREAM[2]	LCDIF_D[12]	UART3_CTS_B	SPI4_PCS2	UART4_CTS_B		3.3V
100	**GPIO_IO17**	GPIO2_IO[17]	SAI3_MCLK	ISI_D[8]	LCDIF_D[13]	UART3_RTS_B	SPI4_PCS1	UART4_RTS_B		3.3V
118	**GPIO_IO18**	GPIO2_IO[18]	SAI3_RX_BCLK	ISI_D[9]	LCDIF_D[14]	SPI5_PCS0	SPI4_PCS0	TPM5_CH2		3.3V
119	**GPIO_IO19**	GPIO2_IO[19]	SAI3_RX_SYNC	PDM_BIT_STREAM[3]	LCDIF_D[15]	SPI5_SIN	SPI4_SIN	TPM6_CH2	SAI3_TX_DATA[0]	3.3V
116	**GPIO_IO20**	GPIO2_IO[20]	SAI3_RX_DATA[0]	PDM_BIT_STREAM[0]	LCDIF_D[16]	SPI5_SOUT	SPI4_SOUT	TPM3_CH1		3.3V
117	**GPIO_IO21**	GPIO2_IO[21]	SAI3_TX_DATA[0]	PDM_CLK	LCDIF_D[17]	SPI5_SCK	SPI4_SCK	TPM4_CH1	SAI3_RX_BCLK	3.3V
115	**GPIO_IO22**	GPIO2_IO[22]	SDIO3_CLK	SPDIF1_IN	LCDIF_D[18]	TPM5_CH1	TPM6_EXTCLK	I2C5_SDA		3.3V
96	**GPIO_IO23**	GPIO2_IO[23]	SDIO3_CMD	SPDIF1_OUT	LCDIF_D[19]	TPM6_CH1		I2C5_SCL		3.3V
99	**GPIO_IO24**	GPIO2_IO[24]	SDIO3_DATA0		LCDIF_D[20]	TPM3_CH3		SPI6_PCS1		3.3V
95	**GPIO_IO25**	GPIO2_IO[25]	SDIO3_DATA1	CAN2_TX	LCDIF_D[21]	TPM4_CH3		SPI7_PCS1		3.3V
47	**GPIO_IO26**	GPIO2_IO[26]	SDIO3_DATA2	PDM_BIT_STREAM[1]	LCDIF_D[22]	TPM5_CH3		SPI8_PCS1	SAI3_TX_SYNC	3.3V
48	**GPIO_IO27**	GPIO2_IO[27]	SDIO3_DATA3	CAN2_RX	LCDIF_D[23]	TPM6_CH3		SPI5_PCS1		3.3V
98	**GPIO_IO28**	GPIO2_IO[28]	I2C3_SDA							3.3V

Pad #	SoC Pin Name	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	Voltage Domain
97	**GPIO_IO29**	GPIO2_IO[29]	I2C3_SCL							3.3V
131	**SAI1_RXD0**	SAI1_RX_DATA[0]	SAI1_MCLK	SPI1_SOUT	UART2_DSR_B	MQS1_RIGHT	GPIO1_IO[14]			3.3V
132	**SAI1_TXC**	SAI1_TX_BCLK	UART2_CTS_B	SPI1_SIN	UART1_DSR_B	CAN1_RX	GPIO1_IO[12]			3.3V
66	**SAI1_TXD0**	SAI1_TX_DATA[0]	UART2_RTS_B	SPI1_SCK	UART1_DTR_B	CAN1_TX	GPIO1_IO[13]/ BOOT_MODE[3]			3.3V
126	**SAI1_TXFS**	SAI1_TX_SYNC	SAI1_TX_DATA[1]	SPI1_PCS0	UART2_DTR_B	MQS1_LEFT	GPIO1_IO[11] /BOOT_MODE[2]			3.3V
74	**SD2_CD_B**	SDIO2_CD_B	ENET_QOS_1588_E VENT0_IN	I3C2_SCL			GPIO3_IO[0]			3.3V/1.8V
70	**SD2_CLK**	SDIO2_CLK	ENET_QOS_1588_E VENT0_OUT	I3C2_SDA			GPIO3_IO[1]			3.3V/1.8V
69	**SD2_CMD**	SDIO2_CMD	ENET2_1588_EVENT 0_IN	I3C2_PUR	I3C2_PUR_B		GPIO3_IO[2]			3.3V/1.8V
72	**SD2_DATA0**	SDIO2_DATA0	ENET2_1588_EVENT 0_OUT	CAN2_TX			GPIO3_IO[3]			3.3V/1.8V
73	**SD2_DATA1**	SDIO2_DATA1	ENET2_1588_EVENT 1_IN	CAN2_RX			GPIO3_IO[4]			3.3V/1.8V
68	**SD2_DATA2**	SDIO2_DATA2	ENET2_1588_EVENT 1_OUT	MQS2_RIGHT			GPIO3_IO[5]			3.3V/1.8V
67	**SD2_DATA3**	SDIO2_DATA3	LPTMR2_ALT1	MQS2_LEFT			GPIO3_IO[6]			3.3V/1.8V
65	**SD2_RESET_B**	SDIO2_RESET_B	LPTMR2_ALT2				GPIO3_IO[7]			3.3V/1.8V
109	**SD3_CLK**	SDIO3_CLK	FLEXSPI_A_SCLK				GPIO3_IO[20]			1.8V
113	**SD3_CMD**	SDIO3_CMD	FLEXSPI_A_SS0_B				GPIO3_IO[21]			1.8V
114	**SD3_DATA0**	SDIO3_DATA0	FLEXSPI_A_DATA[0]				GPIO3_IO[22]			1.8V
112	**SD3_DATA1**	SDIO3_DATA1	FLEXSPI_A_DATA[1]				GPIO3_IO[23]			1.8V
110	**SD3_DATA2**	SDIO3_DATA2	FLEXSPI_A_DATA[2]				GPIO3_IO[24]			1.8V
111	**SD3_DATA3**	SDIO3_DATA3	FLEXSPI_A_DATA[3]				GPIO3_IO[25]			1.8V
64	**UART1_RXD**	UART1_RX		SPI2_SIN	TPM1_CH0		GPIO1_IO[4]			3.3V
63	**UART1_TXD**	UART1_TX		SPI2_PCS0	TPM1_CH1		GPIO1_IO[5]/ BOOT_MODE[0]			3.3V
133	**UART2_RXD**	UART2_RX	UART1_CTS_B	SPI2_SOUT	TPM1_CH2	SAI1_MCLK	GPIO1_IO[6]			3.3V
130	**UART2_TXD**	UART2_TX	UART1_RTS_B	SPI2_SCK	TPM1_CH3		GPIO1_IO[7]/ BOOT_MODE[1]			3.3V

5.7 RTC

MCM-iMX93 features an on-board ultra-low-power AM1805 real time clock (RTC). The RTC is connected to the i.MX93 SoC using I2C2 interface at address 0xD2/D3.

Back-up power supply is required to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about MCM-iMX93 RTC please refer to the AM1805 datasheet.

5.8 Bootstrap Pads

The following MCM-iMX93 pads act as SoC boot-straps and must not be driven during SOM power-up and reset.

Table 60 Bootstrap Signals

Pad#	SoC pin Name	Bootstrap
63	UART1_TXD	BOOT_MODE[0]
66	SAI1_TXD0	BOOT_MODE[3]
126	SAI1_TXFS	BOOT_MODE[2]
130	UART2_TXD	BOOT_MODE[1]

5.9 Reserved Pads

The following MCM-iMX93 pads are reserved and must be left unconnected.

Table 61 Reserved Signals

Pad#
17, 71

6 CARRIER BOARD INTERFACE

MCM-iMX93 carrier board interface uses 140-pin QFN package. SoM pinout is detailed in the following table.

6.1 Package Pinout

Table 62 Package Pinout

Pad #	Pad Functions		Pad #	Pad Functions
1	USB1_ID		71	RESERVED
2	USB1_VBUS_3V3		72	SDIO2_DATA0 ENET2_1588_EVENT0_OUT CAN2_TX GPIO3_IO[3]
3	ONOFF		73	SDIO2_DATA1 ENET2_1588_EVENT1_IN CAN2_RX GPIO3_IO[4]
4	V_SOM		74	SDIO2_CD_B ENET1_1588_EVENT0_IN I3C2_SCL GPIO3_IO[0]
5	ALT_BOOT_USB		75	GND
6	V_SOM		76	ALT_BOOT
7	ADC_IN3		77	JTAG_TDI MQS2_LEFT CAN2_TX GPIO3_IO[28] UART5_RX
8	ADC_IN2		78	JTAG_TMS GPIO3_IO[29] UART5_RTS_B
9	ADC_IN1		79	JTAG_TCLK GPIO3_IO[30] UART5_CTS_B
10	ADC_IN0		80	JTAG_TDO MQS2_RIGHT CAN2_RX GPIO3_IO[31] UART5_TX
11	V_SOM		81	ENET1_TX_CTL UART3_DTR_B GPIO4_IO[6]
12	TAMPER0		82	ENET1_TD1 UART3_RTS_B I3C2_PUR USB1_OTG_OC GPIO4_IO[4] I3C2_PUR_B
13	TAMPER1		83	ENET1_TD2 CAN2_RX USB2_OTG_OC GPIO4_IO[3]
14	SYS_NRST		84	ENET1_TD0 UART3_TX GPIO4_IO[5]
15	V_SOM		85	ENET1_TD3 CAN2_TX USB2_OTG_ID GPIO4_IO[2]
16	PMIC_STBY_REQ		86	ENET1_TXC ENET1_TX_ER GPIO4_IO[7]
17	RESERVED		87	ENET1_RX_CTL UART3_DSR_B

				USB2_OTG_PWR GPIO4_IO[8]
18	CSI_CLK_N		88	ENET1_RD0 UART3_RX GPIO4_IO[10]
19	CSI_CLK_P		89	ENET1_RXC ENET1_RX_ER GPIO4_IO[9]
20	CSI_D0_P		90	ENET1_RD1 UART3_CTS_B LPTMR2_ALT1 GPIO4_IO[11]
21	CSI_D0_N		91	ENET1_RD2 LPTMR2_ALT2 GPIO4_IO[12]
22	CSI_D1_P		92	ENET1_RD3 LPTMR2_ALT3 GPIO4_IO[13]
23	CSI_D1_N		93	ENET1_MDIO UART3_RIN_B I3C2_SDA USB1_OTG_PWR GPIO4_IO[1]
24	DSI_CLK_N		94	ENET1_MDC UART3_DCB_B I3C2_SCL USB1_OTG_ID GPIO4_IO[0]
25	DSI_CLK_P		95	GPIO2_IO[25] SDIO3_DATA1 CAN2_TX LCDIF_D[21] TPM4_CH3 SPI7_PCS1
26	DSI_D3_P		96	GPIO2_IO[23] SDIO3_CMD SPDIF1_OUT LCDIF_D[19] TPM6_CH1 I2C5_SCL
27	DSI_D3_N		97	GPIO2_IO[29] I2C3_SCL
28	DSI_D2_N		98	GPIO2_IO[28] I2C3_SDA
29	DSI_D2_P		99	GPIO2_IO[24] SDIO3_DATA0 LCDIF_D[20] TPM3_CH3 SPI6_PCS1
30	DSI_D1_N		100	GPIO2_IO[17] SAI3_MCLK ISI_D[8] LCDIF_D[13] UART3_RTS_B SPI4_PCS1 UART4_RTS_B
31	DSI_D1_P		101	GPIO2_IO[16] SAI3_TX_BCLK PDM_BIT_STREAM[2] LCDIF_D[12] UART3_CTS_B SPI4_PCS2 UART4_CTS_B
32	DSI_D0_N		102	GPIO2_IO[14] UART3_TX ISI_D[6] LCDIF_D[10] SPI8_SOUT UART8_CTS_B UART4_TX

33	DSI_D0_P		103	GPIO2_IO[15] UART3_RX ISI_D[7] LCDIF_D[11] SPI8_SCK UART8_RTS_B UART4_RX
34	LVDS_TX0_N		104	GPIO2_IO[13] TPM4_CH2 PDM_BIT_STREAM[3] LCDIF_D[9] SPI8_SIN UART8_RX I2C8_SCL
35	LVDS_TX0_P		105	GPIO2_IO[12] TPM3_CH2 PDM_BIT_STREAM[2] LCDIF_D[8] SPI8_PCS0 UART8_TX I2C8_SDA SAI3_RX_SYNC
36	LVDS_TX1_N		106	GPIO2_IO[7] SPI3_PCS1 ISI_D[1] LCDIF_D[3] SPI7_SCK UART6_RTS_B I2C7_SCL
37	LVDS_TX1_P		107	GPIO2_IO[6] TPM5_CH0 PDM_BIT_STREAM[1] LCDIF_D[2] SPI7_SOUT UART6_CTS_B I2C7_SDA
38	LVDS_CLK_N		108	GPIO2_IO[3] I2C4_SCL ISI_LINE_VALID LCDIF_HSYNC SPI6_SCK UART5_RTS_B I2C6_SCL
39	LVDS_CLK_P		109	SDIO3_CLK FLEXSPI_A_SCLK GPIO3_IO[20]
40	LVDS_TX2_N		110	SDIO3_DATA2 FLEXSPI_A_DATA[2] GPIO3_IO[24]
41	LVDS_TX2_P		111	SDIO3_DATA3 FLEXSPI_A_DATA[3] GPIO3_IO[25]
42	LVDS_TX3_N		112	SDIO3_DATA1 FLEXSPI_A_DATA[1] GPIO3_IO[23]
43	LVDS_TX3_P		113	SDIO3_CMD FLEXSPI_A_SS0_B GPIO3_IO[21]
44	PMIC_ON_REQ		114	SDIO3_DATA0 FLEXSPI_A_DATA[0] GPIO3_IO[22]
45	GPIO2_IO[1] I2C3_SCL ISI_D[0] LCDIF_DE SPI6_SIN UART5_RX I2C5_SCL		115	GPIO2_IO[22] SDIO3_CLK SPDIF1_IN LCDIF_D[18] TPM5_CH1 TPM6_EXTCLK I2C5_SDA
46	POR_B_3P3		116	GPIO2_IO[20] SAI3_RX_DATA[0]

				PDM_BIT_STREAM[0] LCDIF_D[16] SPI5_SOUT SPI4_SOUT TPM3_CH1
47	GPIO2_IO[26] SDIO3_DATA2 PDM_BIT_STREAM[1] LCDIF_D[22] TPM5_CH3 SPI8_PCS1 SAI3_TX_SYNC		117	GPIO2_IO[21] SAI3_TX_DATA[0] PDM_CLK LCDIF_D[17] SPI5_SCK SPI4_SCK TPM4_CH1 SAI3_RX_BCLK
48	GPIO2_IO[27] SDIO3_DATA3 CAN2_RX LCDIF_D[23] TPM6_CH3 SPI5_PCS1		118	GPIO2_IO[18] SAI3_RX_BCLK ISI_D[9] LCDIF_D[14] SPI5_PCS0 SPI4_PCS0 TPM5_CH2
49	ENET2_MDIO UART4_RIN_B SAI2_RX_BCLK GPIO4_IO[15]		119	GPIO2_IO[19] SAI3_RX_SYNC PDM_BIT_STREAM[3] LCDIF_D[15] SPI5_SIN SPI4_SIN TPM6_CH2 SAI3_TX_DATA[0]
50	ENET2_MDC UART4_DCB_B SAI2_RX_SYNC GPIO4_IO[14]		120	GPIO2_IO[8] SPI3_PCS0 ISI_D[2] LCDIF_D[4] TPM6_CH0 UART7_TX I2C7_SDA
51	ENET2_TD3 SAI2_RX_DATA[0] GPIO4_IO[16]		121	GPIO2_IO[9] SPI3_SIN ISI_D[3] LCDIF_D[5] TPM3_EXTCLK UART7_RX I2C7_SCL
52	ENET2_TD0 UART4_TX SAI2_RX_DATA[3] GPIO4_IO[19]		122	GPIO2_IO[11] SPI3_SCK ISI_D[5] LCDIF_D[7] TPM5_EXTCLK UART7_RTS_B I2C8_SCL
53	ENET2_TD1 UART4_RTS_B SAI2_RX_DATA[2] GPIO4_IO[18]		123	GPIO2_IO[10] SPI3_SOUT ISI_D[4] LCDIF_D[6] TPM4_EXTCLK UART7_CTS_B I2C8_SDA
54	ENET2_TX_CTL UART4_DTR_B SAI2_TX_SYNC GPIO4_IO[20]		124	GPIO2_IO[5] TPM4_CH0 PDM_BIT_STREAM[0] LCDIF_D[1] SPI7_SIN UART6_RX I2C6_SCL
55	ENET2_TD2 SAI2_RX_DATA[1] GPIO4_IO[17]		125	GPIO2_IO[4] TPM3_CH0 PDM_CLK LCDIF_D[0] SPI7_PCS0 UART6_TX I2C6_SDA

56	ENET2_TXC ENET2_TX_ER SAI2_TX_BCLK GPIO4_IO[21]		126	SAI1_TX_SYNC SAI1_TX_DATA[1] SPI1_PCS0 UART2_DTR_B MQS1_LEFT GPIO1_IO[11]/BOOT_MODE[2]
57	ENET2_RXC ENET2_RX_ER SAI2_TX_DATA[1] GPIO4_IO[23]		127	VCC_RTC
58	ENET2_RX_CTL UART4_DSR_B SAI2_TX_DATA[0] GPIO4_IO[22]		128	GPIO2_IO[2] I2C4_SDA ISI_FRAME_VALID LCDIF_VSYNC SPI6_SOUT UART5_CTS_B I2C6_SDA
59	ENET2_RD0 UART4_RX SAI2_TX_DATA[2] GPIO4_IO[24]		129	GPIO2_IO[0] I2C3_SDA ISI_PCLK LCDIF_PCLK SPI6_PCS0 UART5_TX I2C5_SDA
60	ENET2_RD1 SPDIF1_IN SAI2_TX_DATA[3] GPIO4_IO[25]		130	UART2_TX UART1_RTS_B SPI2_SCK TPM1_CH3 GPIO1_IO[7]/BOOT_MODE[1]
61	ENET2_RD2 UART4_CTS_B SAI2_MCLK MQS2_RIGHT GPIO4_IO[26]		131	SAI1_RX_DATA[0] SAI1_MCLK SPI1_SOUT UART2_DSR_B MQS1_RIGHT GPIO1_IO[14]
62	ENET2_RD3 SPDIF1_OUT SPDIF1_IN MQS2_LEFT GPIO4_IO[27]		132	SAI1_TX_BCLK UART2_CTS_B SPI1_SIN UART1_DSR_B CAN1_RX GPIO1_IO[12]
63	UART1_TX SPI2_PCS0 TPM1_CH1 GPIO1_IO[5]/BOOT_MODE[0]		133	UART2_RX UART1_CTS_B SPI2_SOUT TPM1_CH2 SAI1_MCLK GPIO1_IO[6]
64	UART1_RX SPI2_SIN TPM1_CH0 GPIO1_IO[4]		134	VSD_3V3
65	SDIO2_RESET_B LPTMR2_ALT2 GPIO3_IO[7]		135	USB2_ID
66	SAI1_TX_DATA[0] UART2_RTS_B SPI1_SCK UART1_DTR_B CAN1_TX GPIO1_IO[13]/BOOT_MODE[3]		136	USB2_DP
67	SDIO2_DATA3 LPTMR2_ALT1 MQS2_LEFT GPIO3_IO[6]		137	USB2_DN
68	SDIO2_DATA2 ENET2_1588_EVENT1_OUT MQS2_RIGHT GPIO3_IO[5]		138	USB2_VBUS_3V3
69	SDIO2_CMD ENET2_1588_EVENT0_IN		139	USB1_DP

	I3C2_PUR I3C2_PUR_B GPIO3_IO[2]			
70	SDIO2_CLK ENET1_1588_EVENT0_OUT I3C2_SDA GPIO3_IO[1]		140	USB1_DN

Table 63 Ground Pads

Pad #	Pad Functions		Pad #	Pad Functions
G1	GND		G15	GND
G2			G16	
G3			G17	
G4			G18	
G5			G19	
G6			G20	
G7			G21	
G8			G22	
G9			G23	
G10			G24	
G11			G25	
G12			G26	
G13			G27	
G14			G28	

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 64 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	6.0	V
Voltage on any non-power supply pin	-0.5	3.6	V
Backup battery supply voltage (VCC_RTC)	-0.3	3.8	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 65 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.45	3.7	5.5	V
Backup battery supply voltage (VCC_RTC)	1.5	3.0	3.6	V

7.3 Typical Power Consumption

Table 66 OFF Power Consumption

Use case	Use case description	I_{SOM}	P_{SOM}
OFF mode	Linux shutdown / power-off	1mA	

Table 67 RTC timekeeping current

Use case	Use case description	I_{VCC_RTC}
RTC only	VCC_RTC (3.0V) is supplied from external coin-cell battery V_SOM is not present	70nA

7.4 ESD Performance

Table 68 ESD Performance

Interface	ESD Performance
i.MX93 pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)

8 MECHANICAL SPECIFICATIONS

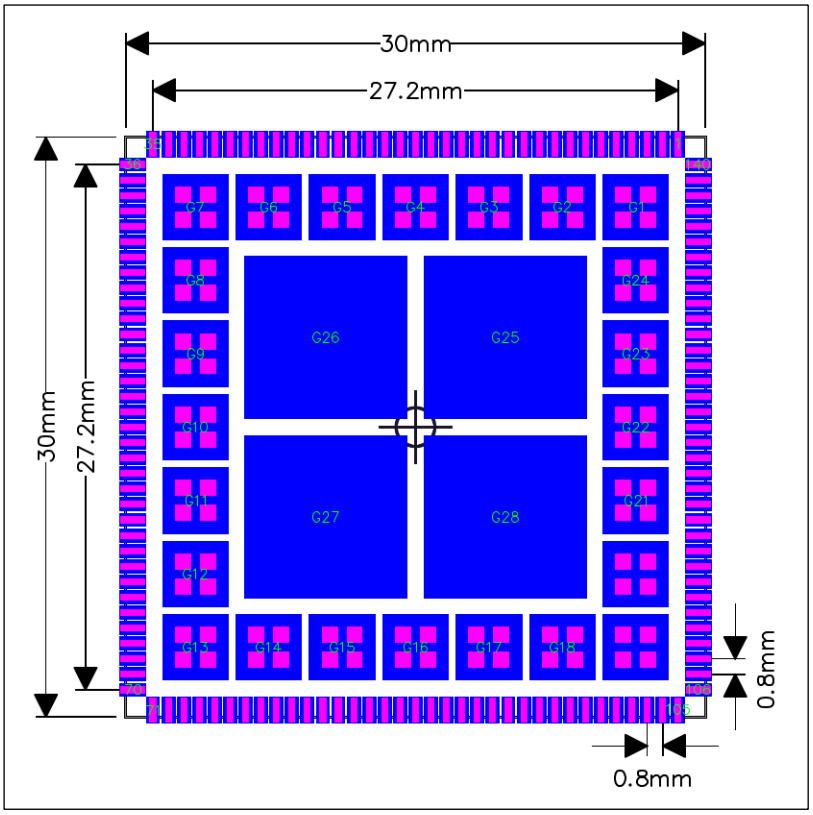
8.1 Mechanical Drawings

3D model and mechanical drawings in DXF format are available at

https://www.compulab.com/products/computer-on-modules/mcm-imx93-nxp-i-mx-93-som-smd-system-on-module/#devres

8.2 Recommended Footprint

Figure 3 MCM-iMX93 footprint



NOTE: solder paste must not be applied to center ground pads G25, G26, G27, G28. These pads should remain unsoldered.

MCM-iMX8M-Mini footprint in DXF and HKP formats is available at

https://www.compulab.com/products/computer-on-modules/mcm-imx93-nxp-i-mx-93-som-smd-system-on-module/#devres

9 APPLICATION NOTES

9.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V_SOM and GND near the SOM.
- Except for a power connection, no other connection is mandatory for MCM-iMX93 operation. All power-up circuitry and all required pullups/pulldowns are available onboard MCM-iMX93.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- Refer to the SB-MCMIMX93 carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

9.2 Carrier Board Troubleshooting

- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches.
- Using an oscilloscope, verify that the SOM GND pins are indeed at zero voltage level and that there is no ground bouncing.
- Create a "minimum system" - only power, the SOM and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
  - External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
  - Faulty power supply
  - To avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.

- Check for the existence of soldering shorts between the SOM pads. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.