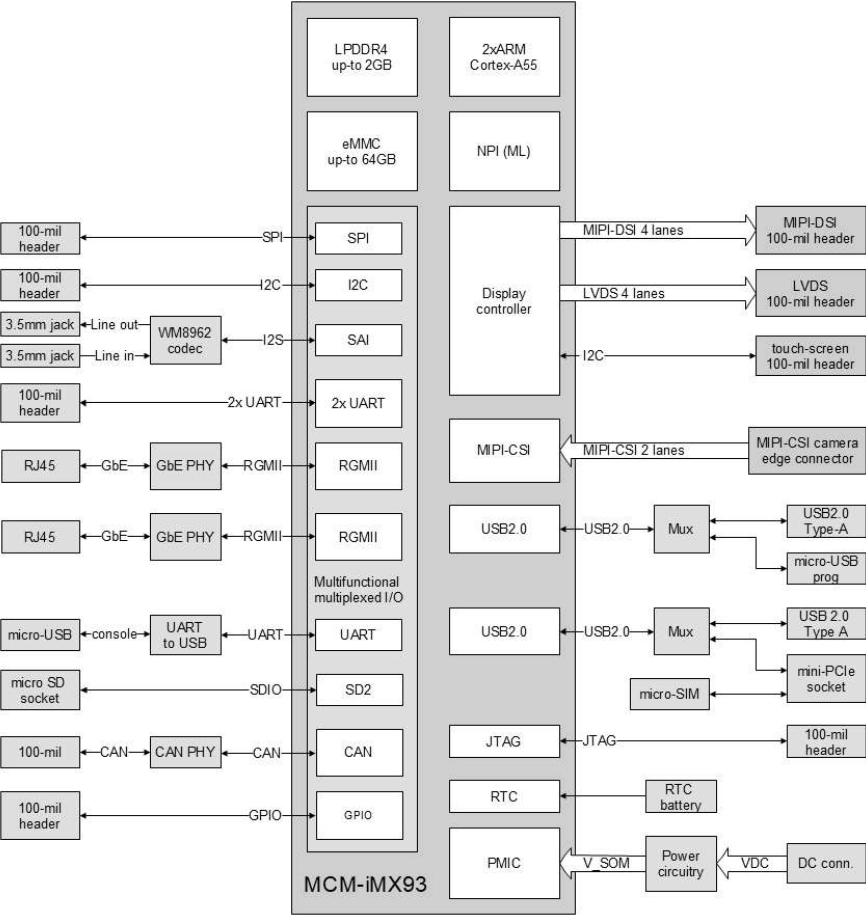


SBC-MCM93

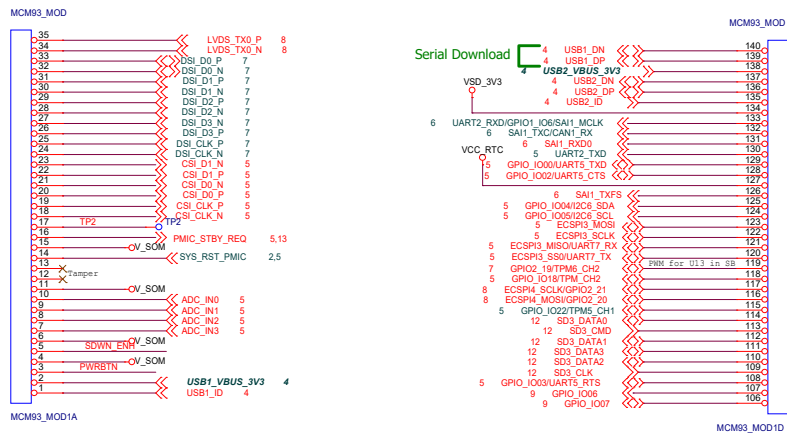
BOARD REVISION: 1.0

Page	Description
01	Index and Block Diagram
02	MCM Connectors
03	DC INP, Discharge
04	USB
05	JTAG, SPDIF,CAN, CSI,MISC
06	Codec
07	MIPI-DSI LCD
08	LVDS LCD
09	GBE
10	Ethernet connectos
11	Console, RS232, SD, miniPCIe
12	WIFI&Bluetooth
13	Power
14	Mechanical

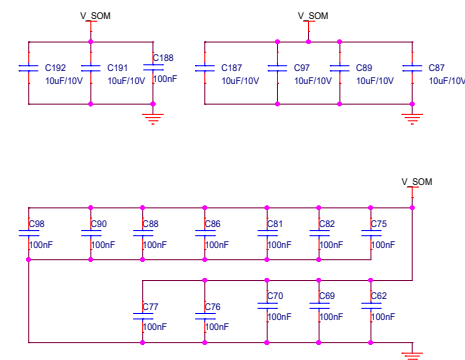
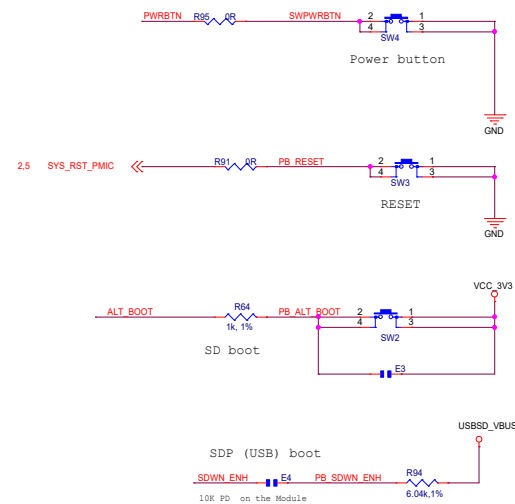


PCB1
PCB, SBC-MCM93, Rev 1.0
PIN = 188C04590

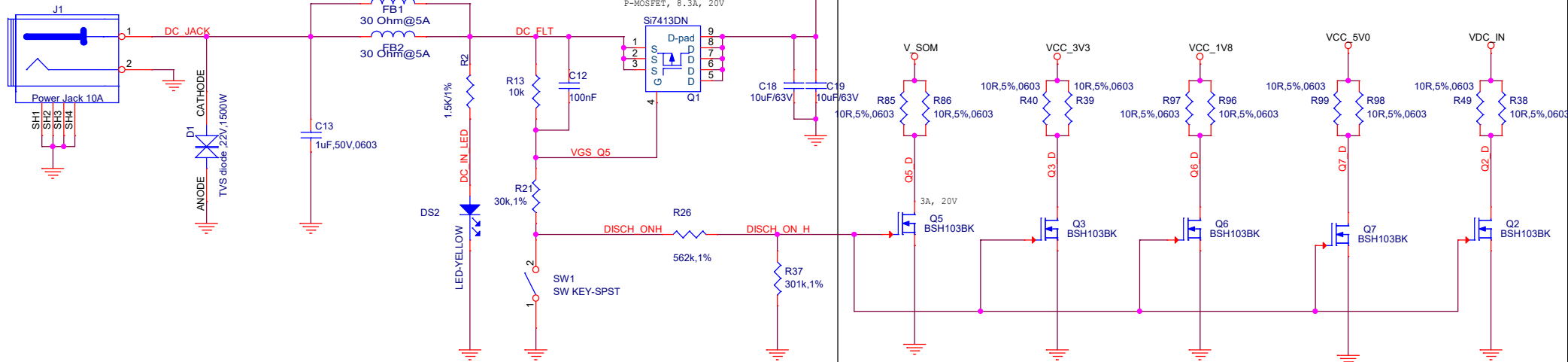
ZZ1
PARSER_VERSION_1.0



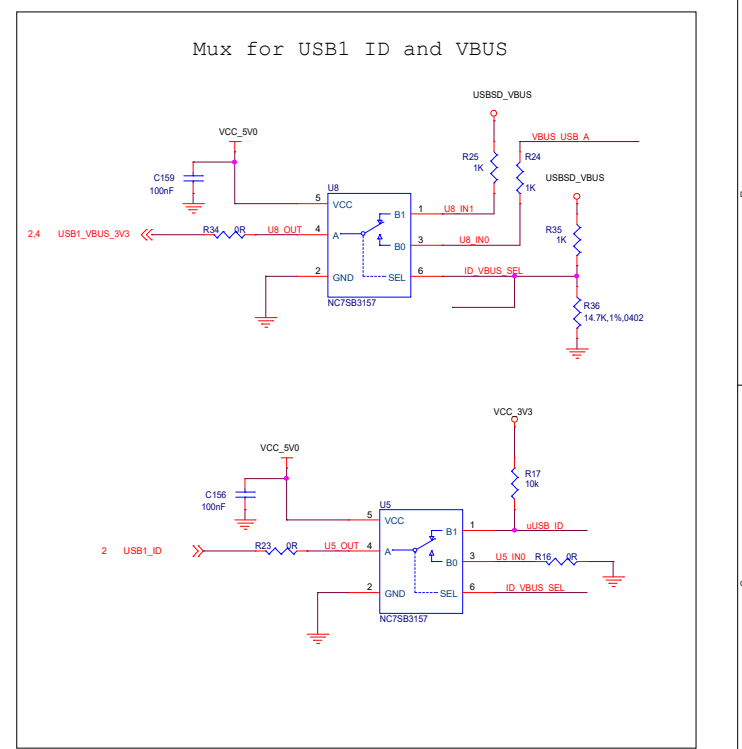
MCM connectors



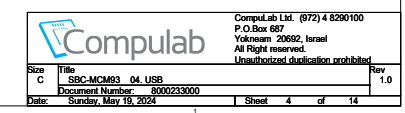
DC input
 $V_{in} = 8V-18V$
 $I_{max} (V_{in}=10V) = 3.31A$

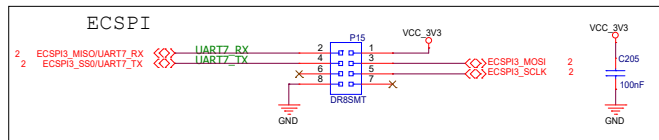
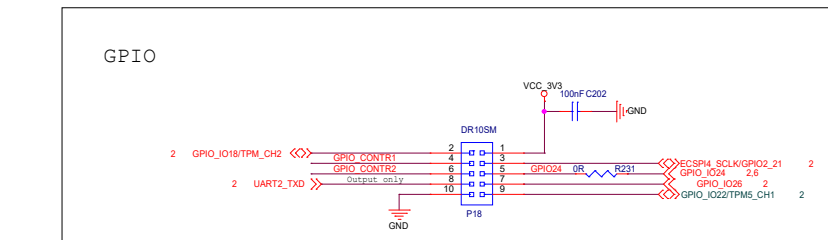
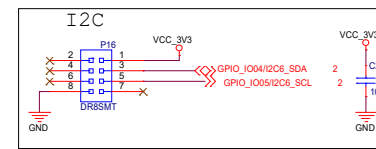
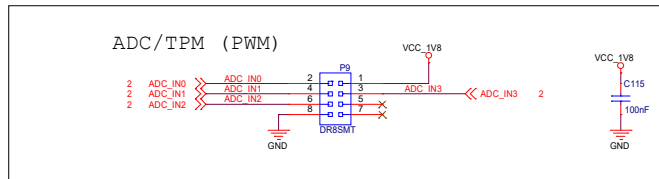
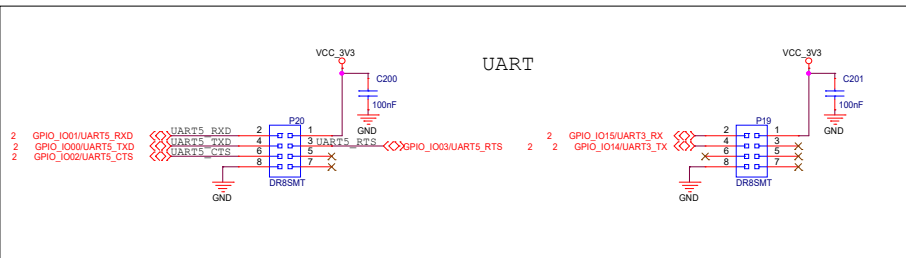
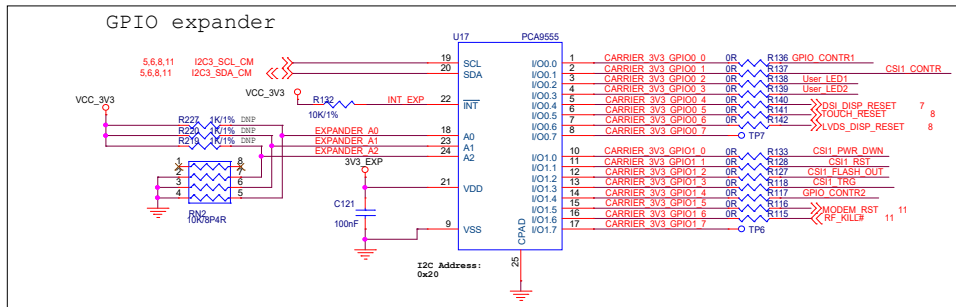
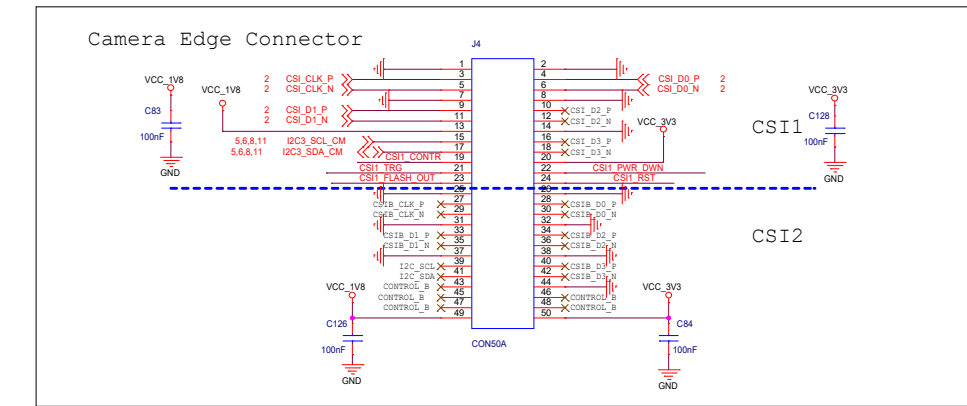
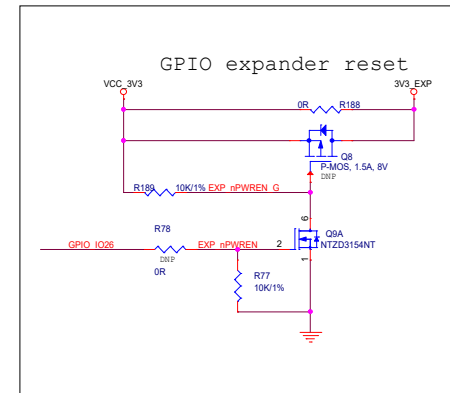
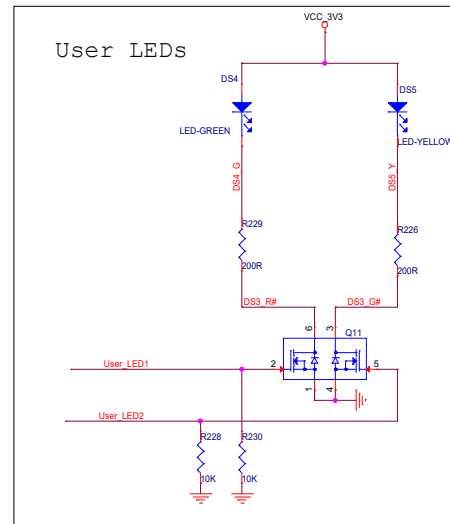
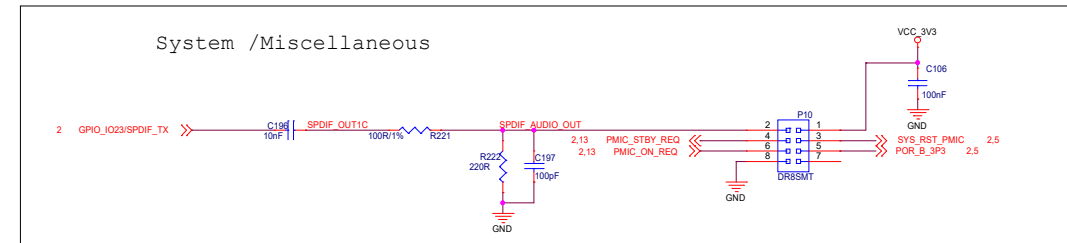
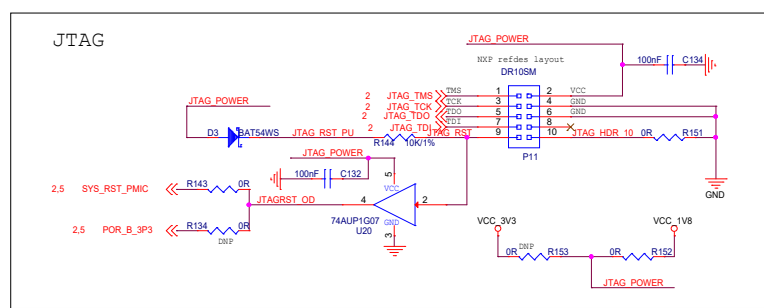
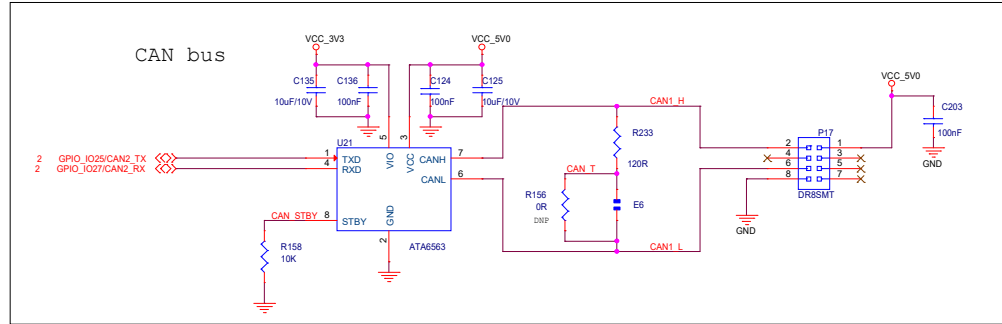


NOTE: USB1 multiplexing is controlled by presence of VBUS on connector P21

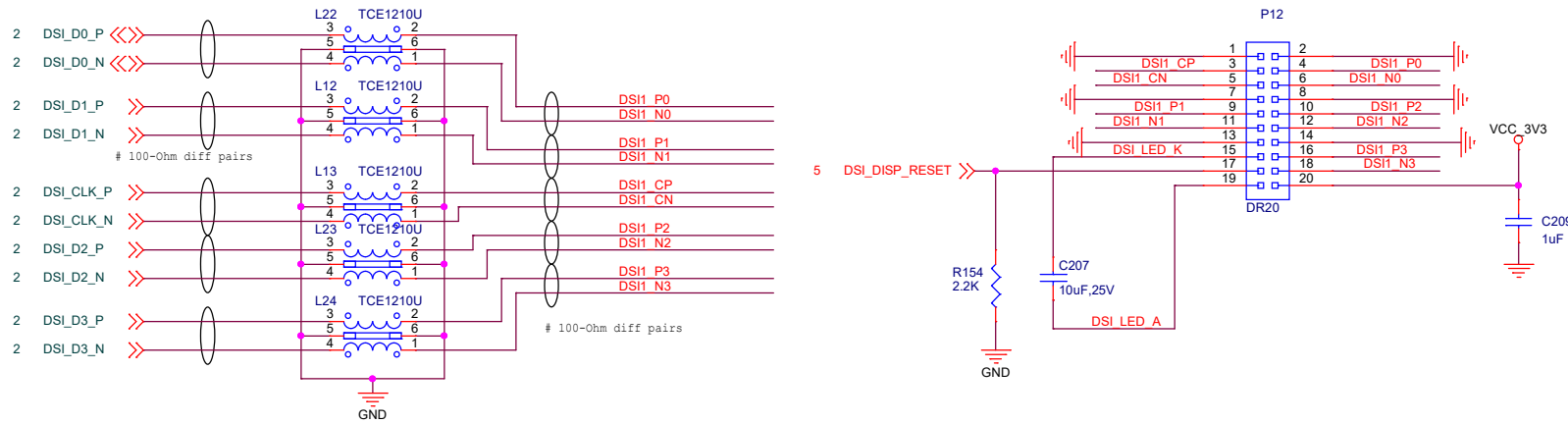


NOTE: USB1 multiplexing is controlled by jumper E1



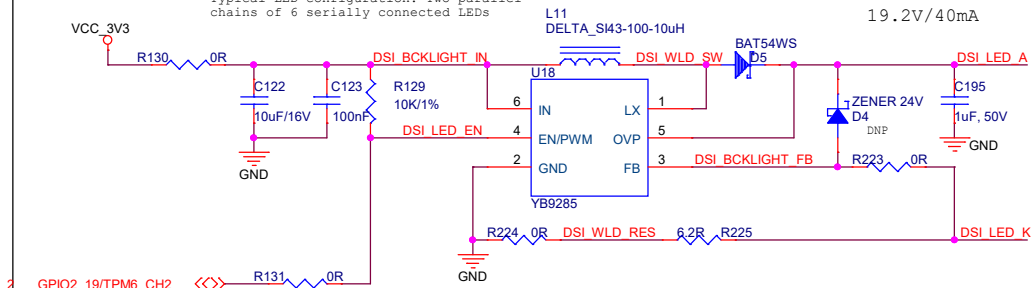


MIPI-DSI LCD Int.

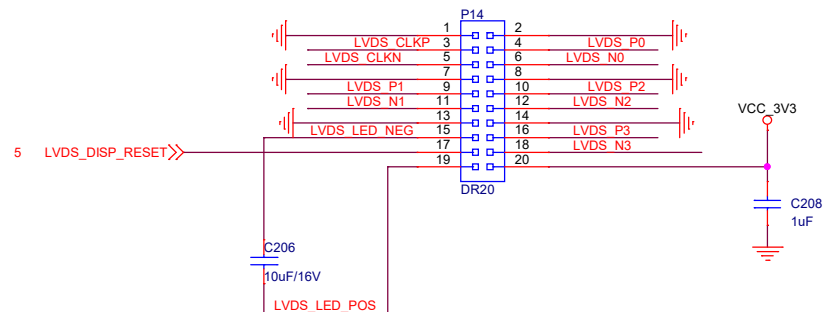
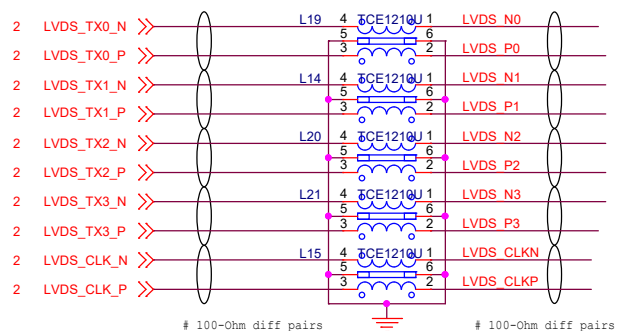


MIPI LCD back-light power

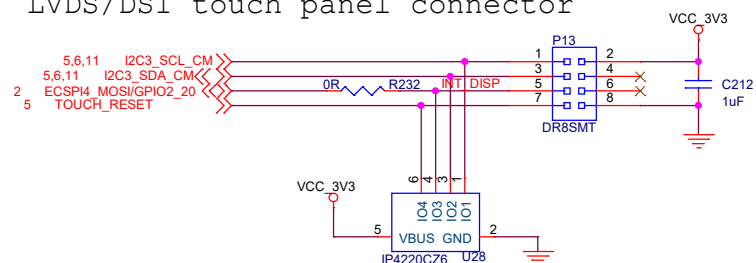
Typical LED configuration: Two parallel chains of 6 serially connected LEDs



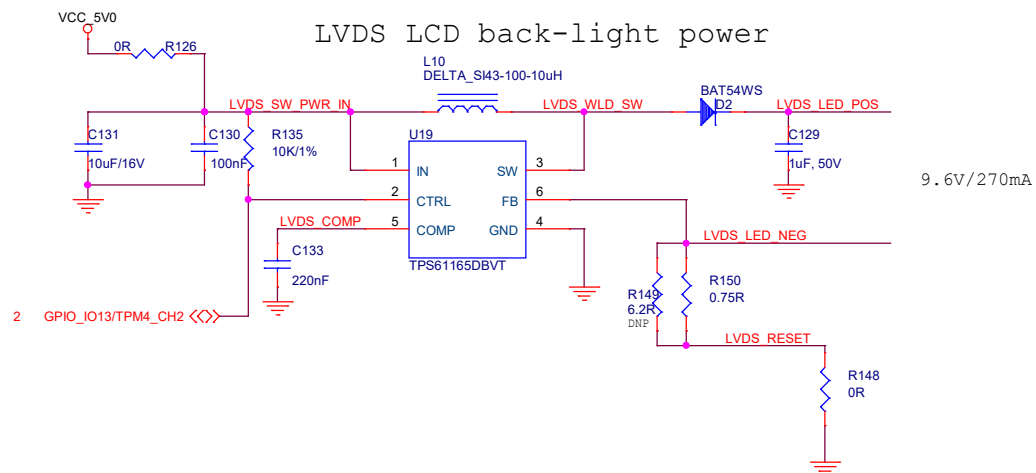
LVDS LCD Int.



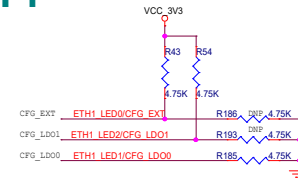
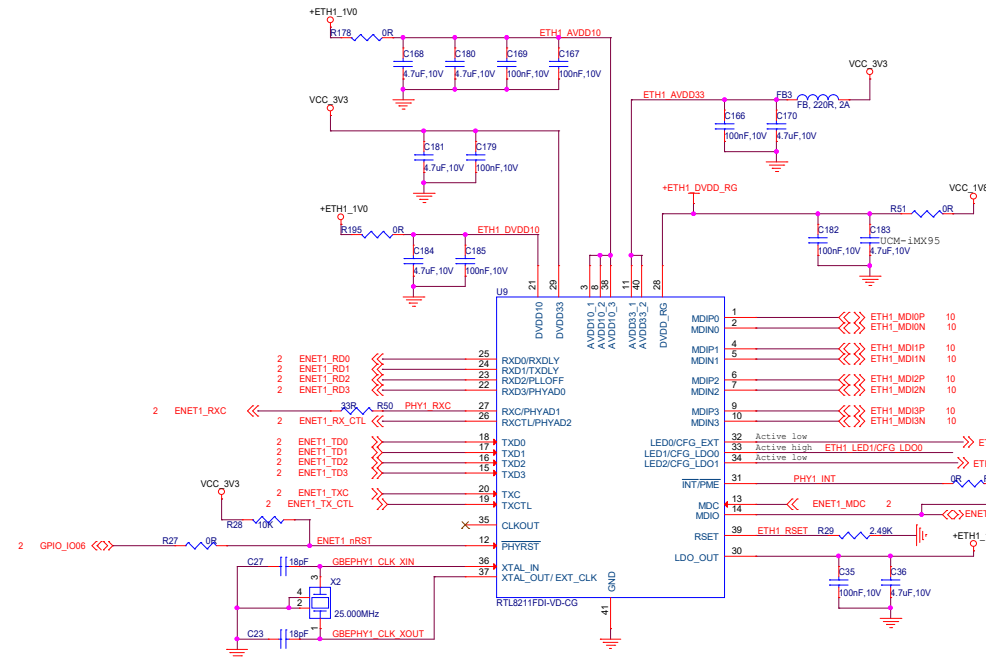
LVDS/DSI touch panel connector



LVDS LCD back-light power

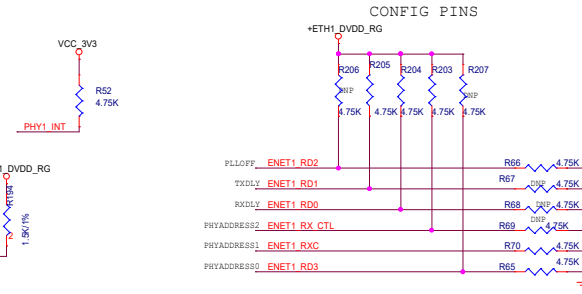


		CompuLab Ltd. (972) 4 8290100 P.O.Box 687 Yokneam 20692, Israel All Right reserved. Unauthorized duplication prohibited	
		Size B Title SBC-MCM93 08. LVDS LCD Document Number: 8000233000 Date: Sunday, May 19, 2024	Rev 1.0 Sheet 8 of 14

GbE PHY1

Power-on Strapping Pins CFG

PGM1 Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V (Default)	1	00
External 1.8V	1	10
Internal 1.8V	0	10



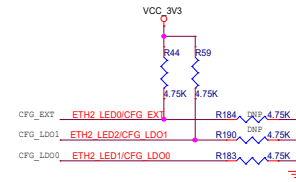
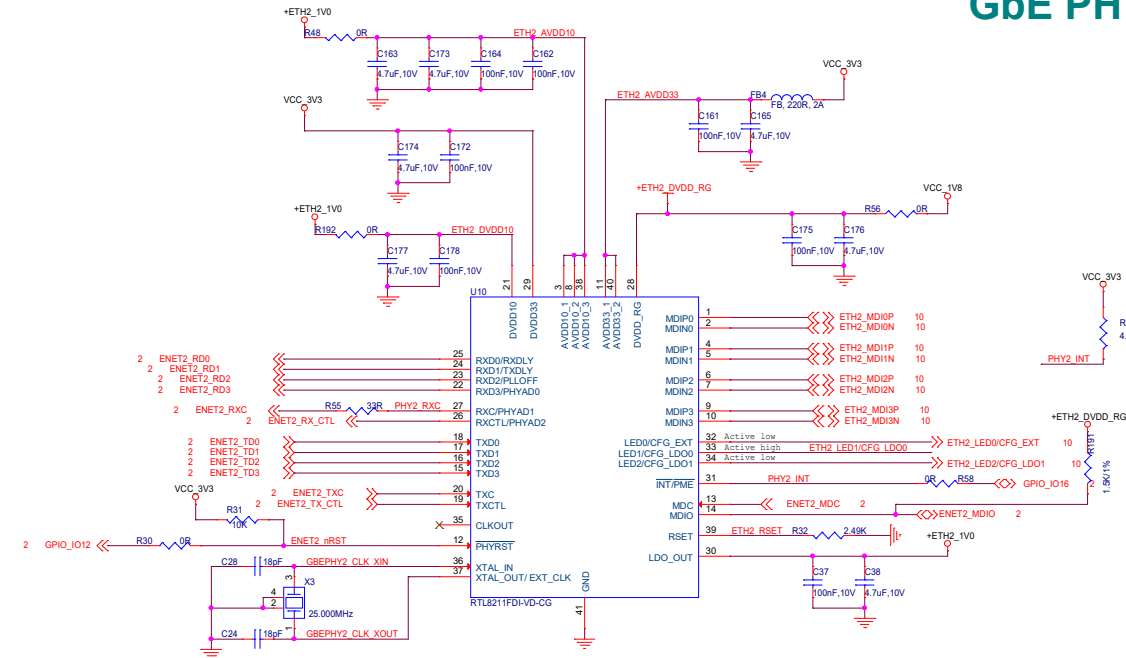
```
PHY ADDRESS = [1,0,0]
PHY support addresses from 00001 to 00111.
PHY address 0 is a broadcast from the MAC

PILLOFF: Pull-up to disable PLL @ ALDPS mod
```

```
Enable internal delays

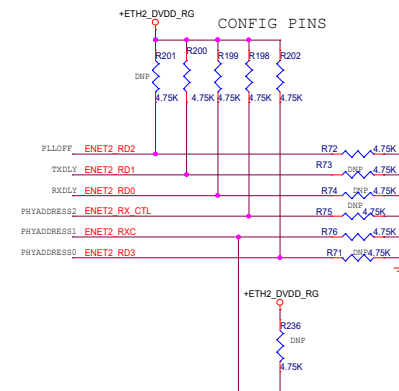
TX delay is enabled
RX delay is enabled
```

GbE PHY2



Power-on Strapping Pins CFG

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V (Default)	1	00
External 1.8V	1	10
Internal 1.8V	0	10

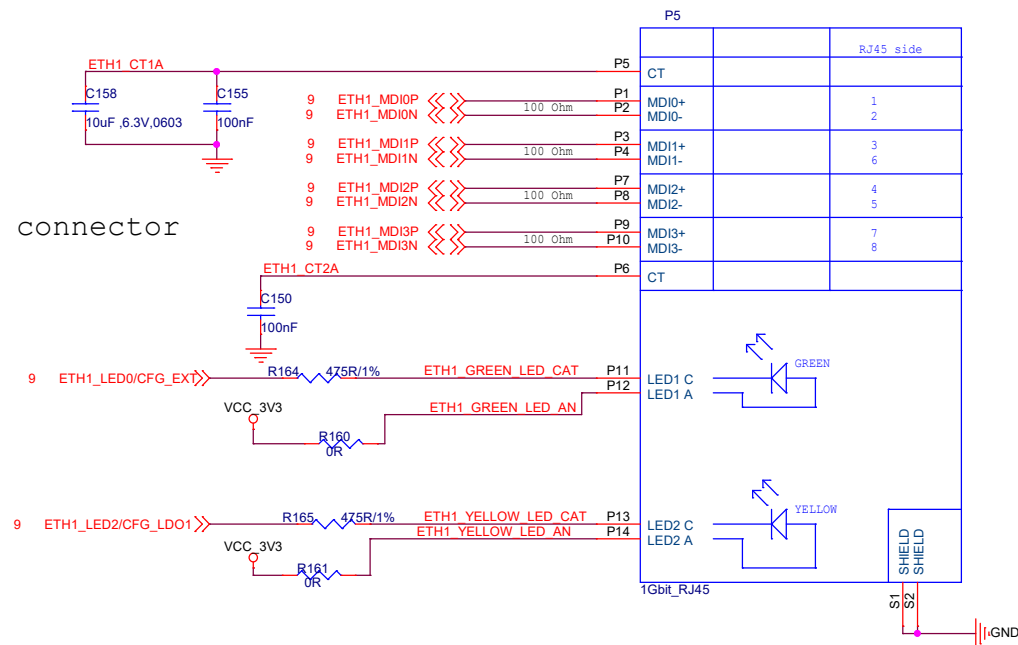


```
PHY ADDRESS = [1,0,1]
PHY support addresses from 00001 to 00111.
PHY address 0 is a broadcast from the MAC

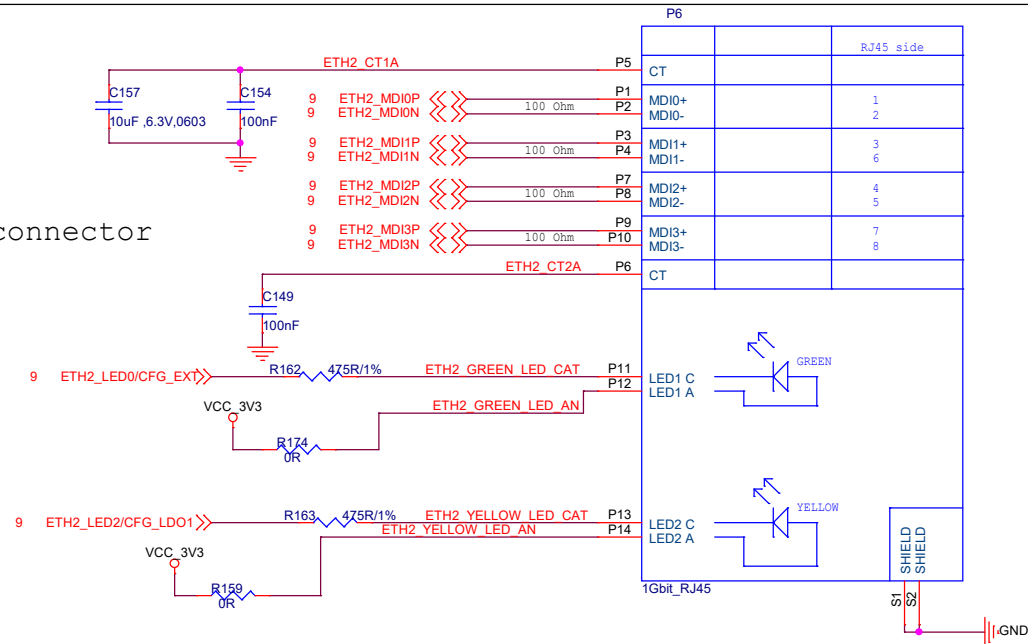
PLLOFF: Pull-up to disable PLL @ ALDPS mo
```

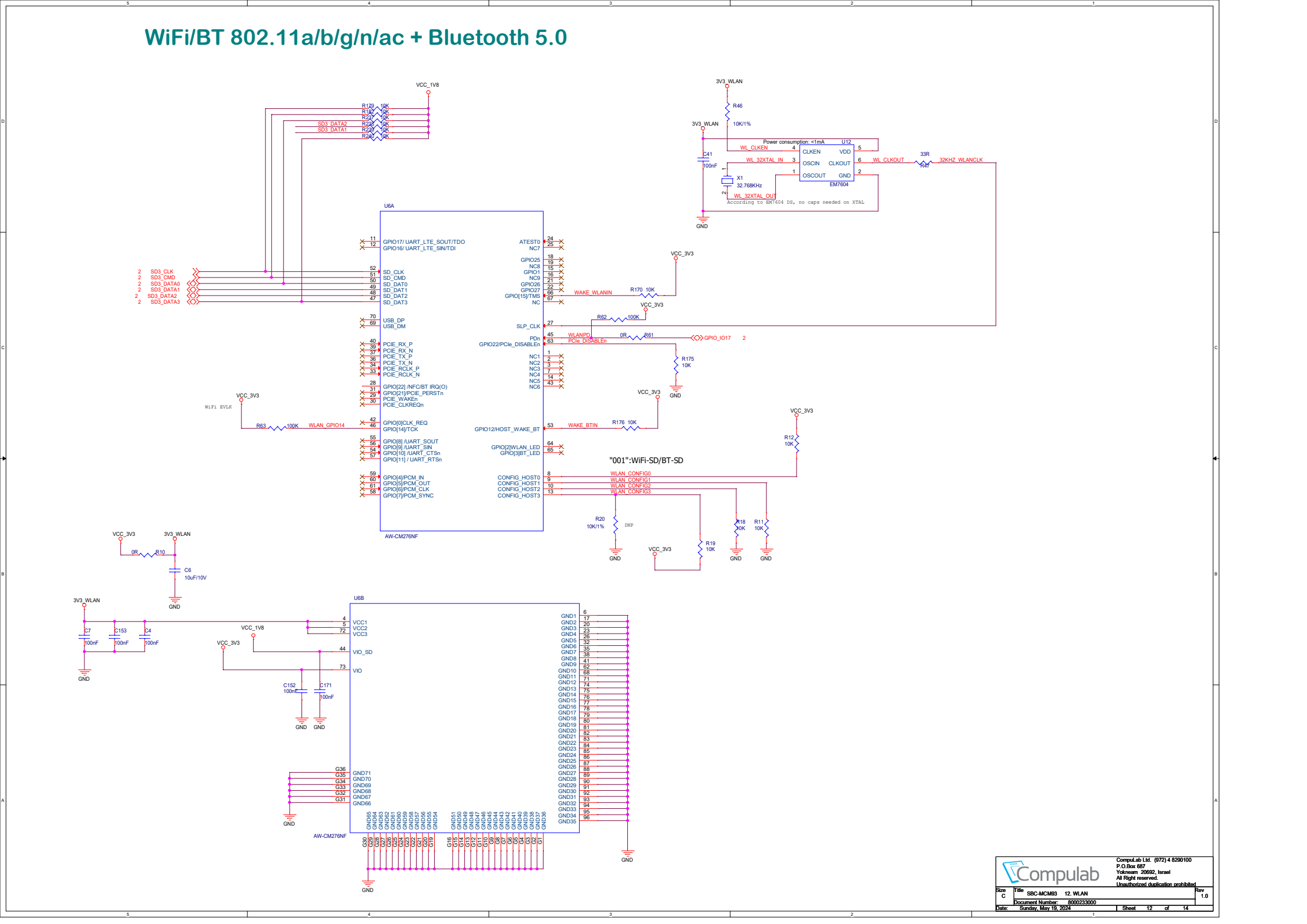
```
Enable internal delays
TX delay is enabled
RX delay is enabled
```

Ethernet 1 connector

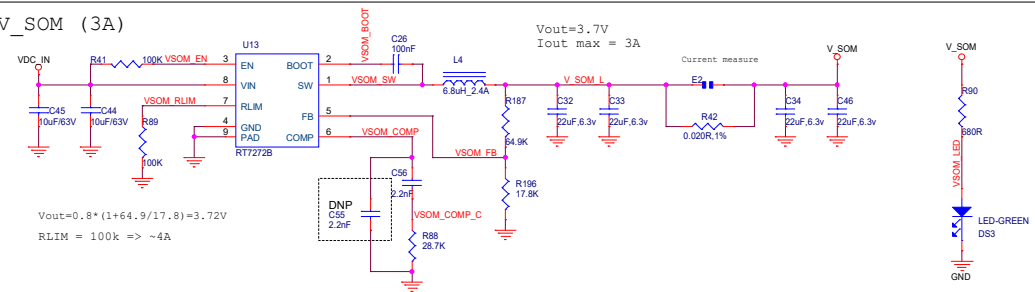


Ethernet 2 connector

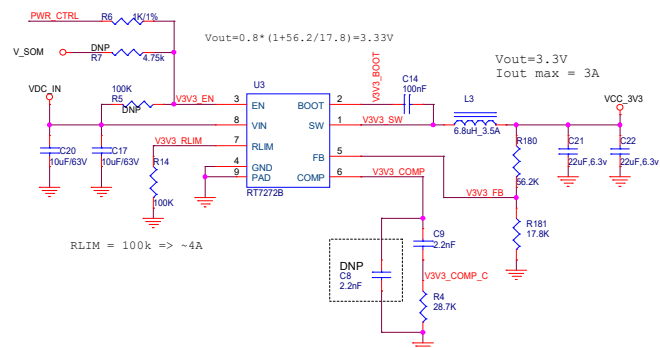




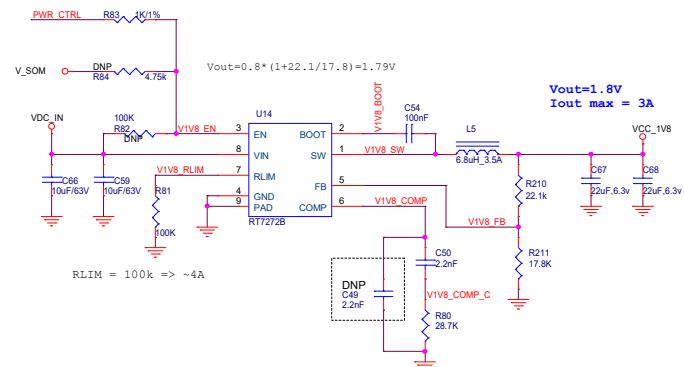
V_SOM (3A)



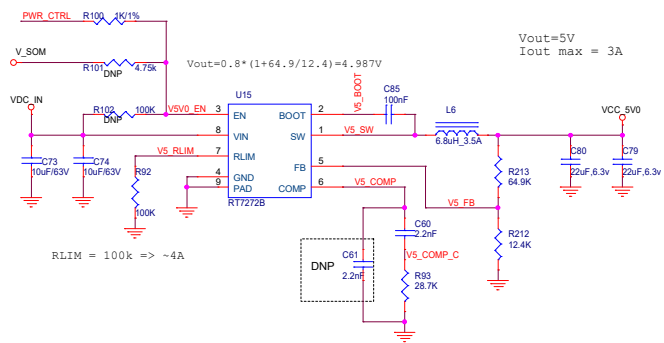
VCC_3V3



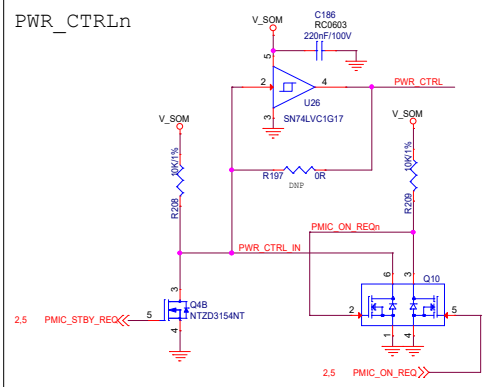
VCC_1V8



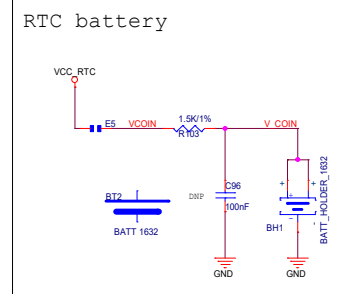
VCC_5V



PWR_CTRLn



RTC battery



SPACER1

SP1 

Through hole diameter should be 2.55mm

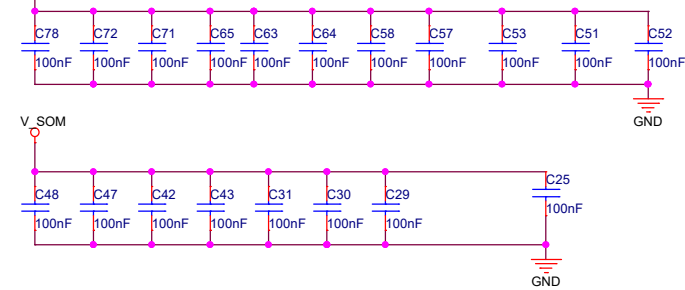
SP2 

SPACER2



GND

VCC_3V3



JP1

JP2

JP3

JP4

JP5

JP6

JP7

Jumper, black, 100mill