MCM-iMX8M-Plus

Reference Guide

Compulab

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Table 1 Revision Notes

Date	Description
Jul 2024	• Initial release

Please check for a newer revision of this manual at the Compulab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

Compulab System on Module (SOM) products are fully featured, miniature board computers designed for integration into custom industrial applications

This document is part of a set of reference documents providing information necessary to operate and program Compulab MCM-iMX8M-Plus System-on-Module.

1.2 MCM-iMX8M-Plus Part Number Legend

Please refer to the Compulab website 'Ordering Info' section to decode the MCM-iMX8M-Plus part number: https://www.compulab.com/products/computer-on-modules/mcm-imx8m-plus-nxp-i-mx-8m-plus-som-system-on-module/#ordering .

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
MCM-iMX8M-Plus Developer Resources	https://www.compulab.com/products/computer-on-modules/mcm-imx8m-plus-nxp-i-mx-8m-plus-som-system-on-module-computer/#devres
i.MX8M Plus Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-plus-arm-cortex-a53-machine-learning-vision-multimedia-and-industrial-iot:IMX8MPLUS?tab=Documentation_Tab
i.MX8M Plus Datasheet	

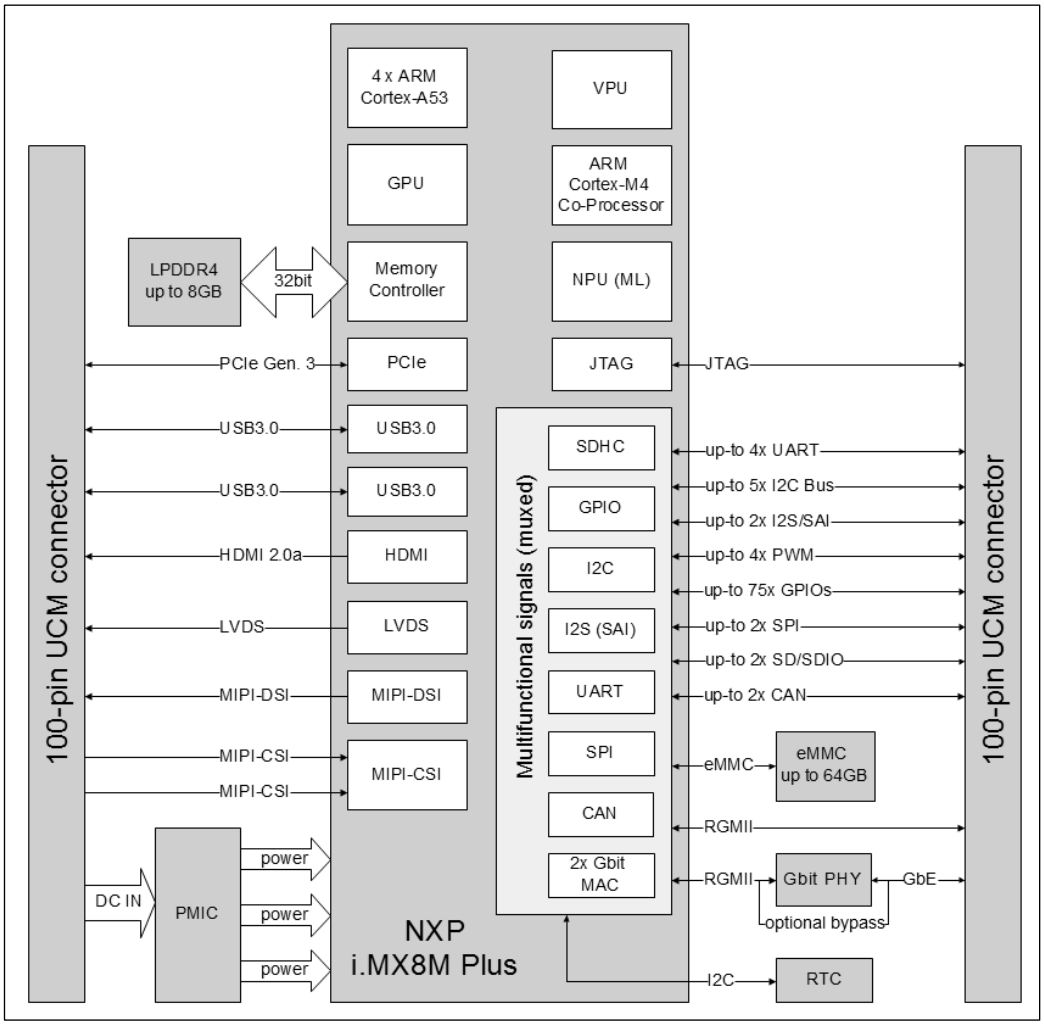
2 OVERVIEW

2.1 Highlights

- NXP i.MX8M Plus Processor, up-to 1.8GHz
- Up to 8GB LPDDR4 and 64GB eMMC
- 2D/3D GPU, 1080p VPU and audio DSP
- Integrated AI/ML Neural Processing Unit
- HDMI, LVDS, MIPI-DSI
- 2x MIPI-CSI camera inputs with dedicated ISP
- PCIe, 2x RGMII, 2x USB3.0
- 2x CAN, 4x UART, 115x GPIO
- Tiny size and weight - 30 x 30 x 5 mm, 5 gram

2.2 Block Diagram

Figure 1 MCM-iMX8M-Plus Block Diagram



2.3 MCM-iMX8M-Plus Specifications

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX8M Plus Quad, quad-core ARM Cortex-A53, 1.8GHz	C1800QM
	NXP i.MX8M Plus Quad, quad-core ARM Cortex-A53, 1.6GHz, industrial temp. grade	C1600QM
	NXP i.MX8M Plus QuadLite, quad-core ARM Cortex-A53, 1.8GHz	C1800Q
Video Decode	1080p60 HEVC/H.265, AVC/H.264, VP9, VP8	C1800QM or C1600QM
Video Encode	1080p60 HEVC/H.265, AVC/H.264	
GPU	GC7000UL (3D): OpenGL ES 3.1/3.0/2.0/1.1, OpenCL 1.1/1.2; GC520L (2D): DirectFB, GDI/DirectDraw	+
NPU	AI/ML Neural Processing Unit, up to 2.3 TOPS	C1800QM or C1600QM
Real-Time Co-processor	ARM Cortex-M7 @ 800 Mhz	+
DSP	Tensilica® HiFi 4 DSP	C1800QM or C1600QM
Memory and Storage		
RAM	1GB – 8GB, LPDDR4	D
Storage	eMMC flash, 16GB - 64GB	N
Display and Camera		
Display	HDMI 2.0a, up to 1080p60	+
	MIPI-DSI, 4 data lanes, up to 1080p60	+
	LVDS, 4 lanes, up to 1366x768 p60	+
Touchscreen	Capacitive touch-screen support through eSPI and I2C interfaces	+
Camera	2x MIPI-CSI, 4 data lanes	+
Network		
Ethernet	2x RGMII	+
Audio		
Digital Audio	Up-to 4x I2S / SAI	+
	eARC	+
	S/PDIF input/output	+
I/O		
PCI Express	PCIe Gen. 3.0 x1	+
USB	2x USB3.0	+
UART	Up to 4x UART	+
CAN bus	Up-to 2x CAN	+
MMC/SD/SDIO	Up to 2x SD/SDIO	+
SPI	Up to 2x SPI	+
I2C	Up to 5x I2C	+
PWM	Up to 4x general purpose PWM signals	+

Feature	Description	Option
GPIO	Up to 115 GPIO (multifunctional signals shared with other functions)	+
System Logic		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

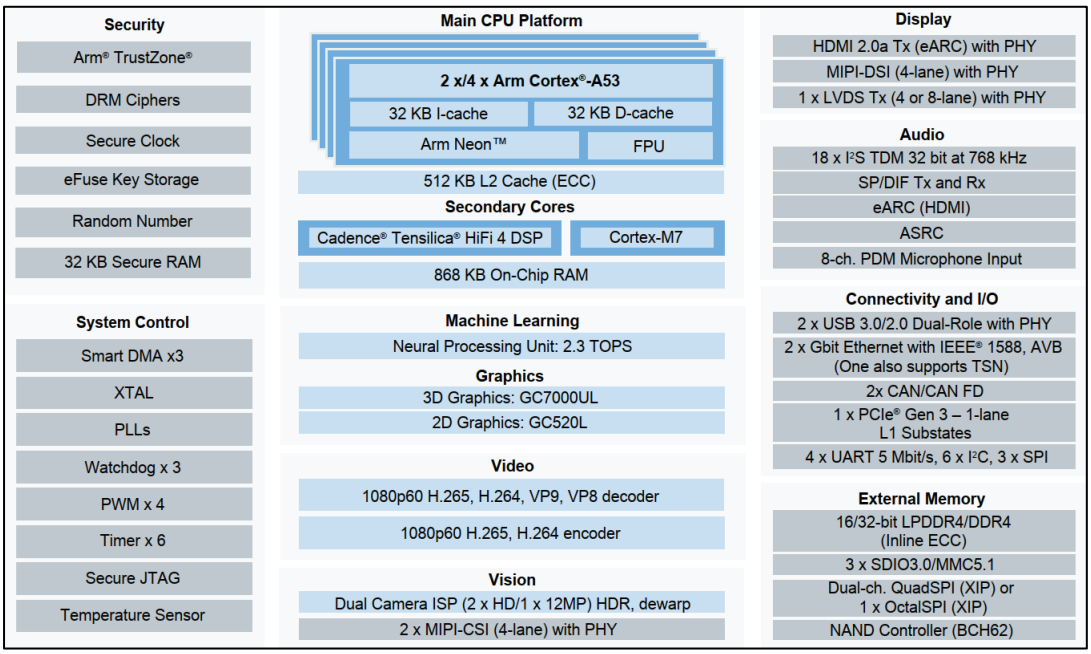
Electrical Specifications	
Supply Voltage	3.45V to 4.4V
Digital I/O voltage	3.3V/1.8V
Mechanical Specifications	
Dimensions	30 x 30 x 3 mm
Weight	5 gram
Foot-print	256-pin, 0.8mm pitch QFN
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 i.MX8M Plus SoC

The i.MX8M Plus family of processors features advanced implementation of a quad ARM® Cortex®-A53 core, which operates at speeds of up to 1.8 GHz. A general purpose Cortex®-M7 core processor enables low-power processing.

Figure 2 i.MX8M Plus Block Diagram



3.2 Memory

3.2.1 DRAM

MCM-iMX8M-Plus is equipped with up to 8GB of onboard LPDDR4 memory. The LPDDR4 channel is 32-bits wide.

3.2.2 Bootloader and General Purpose Storage

MCM-iMX8M-Plus uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is intended to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

MCM-iMX8M-Plus implements a variety of peripheral interfaces through 256-pin carrier board interface pads. The following notes apply to interfaces available through the carrier-board interface:

- Some interfaces/signals are available only with/without certain configuration options of the MCM-iMX8M-Plus SoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Some of the MCM-iMX8M-Plus carrier board interface pins are multifunctional. Up to 4 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.6.
- All of the MCM-iMX8M-Plus digital interfaces operate at 3.3V voltage levels unless noted otherwise.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on MCM-iMX8M-Plus configuration options, certain carrier board interface pins are physically disconnected (floating). The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"P"** – Power
- **"PD" -** Always pulled down onboard MCM-iMX8M-Plus, followed by pull value.
- **"PU" -** Always pulled up onboard MCM-iMX8M-Plus, followed by pull value.
- **"LVDS" -** Low-voltage differential signaling.

4.1 HDMI

The MCM-iMX8M-Plus HDMI interface is implemented with the HDMI interface of the i.MX8M Plus SoC. It supports the following main features:

- Compliant with HDMI 2.0a
- HDMI 2.1 eARC
- Supports display resolutions of up-to 1080p60

The following table summarizes the HDMI interface signals.

Table 5 HDMI Interface Signals

Signal Name	Pin #	Type	Description
HDMI_TXCN	A084	AO	Negative part of HDMI clock diff-pair
HDMI_TXCP	A085	AO	Positive part of HDMI clock diff-pair
HDMI_TX2N	A075	AO	Negative part of HDMI data diff-pair 0
HDMI_TX2P	A076	AO	Positive part of HDMI data diff-pair 0
HDMI_TX1N	A078	AO	Negative part of HDMI data diff-pair 1
HDMI_TX1P	A079	AO	Positive part of HDMI data diff-pair 1
HDMI_TX0N	A081	AO	Negative part of HDMI data diff-pair 2
HDMI_TX0P	A082	AO	Positive part of HDMI data diff-pair 2
HDMI_DDC_SCL	B052	O	VESA Data Display Channel clock
HDMI_DDC_SDA	B053	IO	VESA Data Display Channel data signal
HDMI_HPD	B060	AO	Hot Plug Detect
HDMI_CEC	B061	O	Consumer Electronics Control signal
EARC_N_HPD	B049	AO	
EARC_P_UTIL	B051	AO	

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.2 MIPI-DSI Interface

The MCM-iMX8M-Plus MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX8M Plus SoC. The following main features are supported:

- Scalable data lane support, 1 to 4 data lanes
- Supports MIPI Standard for D-PHY
- Maximum resolution ranges up to Full HD (1920 x 1080 @ 60 Hz)

The table below summarizes the MIPI-DSI interface signals:

Table 6 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description
MIPI_DSI1_CLK_N	A119	AO	Negative part of MIPI-DSI clock diff-pair
MIPI_DSI1_CLK_P	A120	AO	Positive part of MIPI-DSI clock diff-pair
MIPI_DSI1_D0_N	A114	AO	Negative part of MIPI-DSI data diff-pair 0
MIPI_DSI1_D0_P	A115	AO	Positive part of MIPI-DSI data diff-pair 0
MIPI_DSI1_D1_N	A116	AO	Negative part of MIPI-DSI data diff-pair 1
MIPI_DSI1_D1_P	A117	AO	Positive part of MIPI-DSI data diff-pair 1
MIPI_DSI1_D2_N	A122	AO	Negative part of MIPI-DSI data diff-pair 2

Signal Name	Pin #	Type	Description
MIPI_DSI1_D2_P	A123	AO	Positive part of MIPI-DSI data diff-pair 2
MIPI_DSI1_D3_N	A124	AO	Negative part of MIPI-DSI data diff-pair 3
MIPI_DSI1_D3_P	A125	AO	Positive part of MIPI-DSI data diff-pair 3

4.3 LVDS Interface

The MCM-iMX8M-Plus provides one LVDS interface derived from the i.MX8M Plus LVDS display bridge. It supports the following key features:

- Single channel (4 lanes) output at up to 80MHz pixel clock
- Resolutions of up to 1366x768p60

The table below summarizes the LVDS interface signals

Table 7 LVDS Interface Signals

Signal Name	Pin #	Type	Description
LVDS0_CLK_N	B038	AO	Negative part of LVDS clock diff-pair
LVDS0_CLK_P	B037	AO	Positive part of LVDS clock diff-pair
LVDS0_D0_N	B032	AO	Negative part of LVDS data diff-pair 0
LVDS0_D0_P	B031	AO	Positive part of LVDS data diff-pair 0
LVDS0_D1_N	B035	AO	Negative part of LVDS data diff-pair 1
LVDS0_D1_P	B034	AO	Positive part of LVDS data diff-pair 1
LVDS0_D2_N	B041	AO	Negative part of LVDS data diff-pair 2
LVDS0_D2_P	B040	AO	Positive part of LVDS data diff-pair 2
LVDS0_D3_N	B044	AO	Negative part of LVDS data diff-pair 3
LVDS0_D3_P	B043	AO	Positive part of LVDS data diff-pair 3

4.4 Camera Serial Interface

MCM-iMX8M-Plus provides two MIPI-CSI interfaces, both derived from the four-lane MIPI CSI host controller integrated into the i.MX8M Plus SoC with dedicated Image Signal Processor (ISP). The controller supports the following main features:

- Up-to four data lanes and one clock lane
- MIPI D-PHY specification V1.2
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- Image Signal Processor (ISP):
  - Input formats: YCbCr420, YCbCr422, RAW8/10/12/14, RGB444/555/565/666/888
  - Image cropping, de-noising, LS and CA lens correction, AWB

Please refer to the i.MX8M Plus Reference manual for additional details. The following table summarizes MIPI-CSI signals.

Table 8 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description
MIPI_CSI1_CLK_N	A006	AI	Negative part of MIPI-CSI1 clock diff-pair
MIPI_CSI1_CLK_P	A007	AI	Positive part of MIPI-CSI1 clock diff-pair
MIPI_CSI1_D0_N	A011	AI	Negative part of MIPI-CSI1 data diff-pair 0
MIPI_CSI1_D0_P	A012	AI	Positive part of MIPI-CSI1 data diff-pair 0
MIPI_CSI1_D1_N	A009	AI	Negative part of MIPI-CSI11 data diff-pair 1
MIPI_CSI1_D1_P	A010	AI	Positive part of MIPI-CSI1 data diff-pair 1
MIPI_CSI1_D2_N	A003	AI	Negative part of MIPI-CSI1 data diff-pair 2
MIPI_CSI1_D2_P	A004	AI	Positive part of MIPI-CSI1 data diff-pair 2
MIPI_CSI1_D3_N	A001	AI	Negative part of MIPI-CSI1 data diff-pair 3
MIPI_CSI1_D3_P	A002	AI	Positive part of MIPI-CSI1 data diff-pair 3
MIPI_CSI2 _CLK_N	A131	AI	Negative part of MIPI-CSI2 clock diff-pair
MIPI_CSI2 _CLK_P	A132	AI	Positive part of MIPI-CSI2 clock diff-pair
MIPI_CSI2_D0_N	A136	AI	Negative part of MIPI-CSI2 data diff-pair 0
MIPI_CSI2_D0_P	A137	AI	Positive part of MIPI-CSI2 data diff-pair 0
MIPI_CSI2_D1_N	A134	AI	Negative part of MIPI-CSI21 data diff-pair 1
MIPI_CSI2_D1_P	A135	AI	Positive part of MIPI-CSI2 data diff-pair 1
MIPI_CSI2_D2_N	A128	AI	Negative part of MIPI-CSI2 data diff-pair 2
MIPI_CSI2_D2_P	A129	AI	Positive part of MIPI-CSI2 data diff-pair 2
MIPI_CSI2_D3_N	A126	AI	Negative part of MIPI-CSI2 data diff-pair 3
MIPI_CSI2_D3_P	A127	AI	Positive part of MIPI-CSI2 data diff-pair 3

4.5 RGMII

MCM-iMX8M-Plus features two RMGII interfaces.

The tables below summarize the RGMII interface signals.

Table 9 Primary RGMII ENET Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ENET_MDC	A061	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	ENET_VIO
ENET_MDIO	A060	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	ENET_VIO
ENET0_RD0	A067	I	Ethernet input data from the PHY	ENET_VIO
ENET0_RD1	A066	I	Ethernet input data from the PHY	ENET_VIO
ENET0_RD2	A063	I	Ethernet input data from the PHY	ENET_VIO
ENET0_RD3	A062	I	Ethernet input data from the PHY	ENET_VIO
ENET0_RX_CTL	A065	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	ENET_VIO
ENET0_RXC	A064	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	ENET_VIO
ENET0_TD0	A070	O	Ethernet output data to PHY	ENET_VIO
ENET0_TD1	A068	O	Ethernet output data to PHY	ENET_VIO
ENET0_TD2	A072	O	Ethernet output data to PHY	ENET_VIO

Signal Name	Pin #	Type	Description	Voltage Domain
ENET0_TD3	A069	O	Ethernet output data to PHY	ENET_VIO
ENET0_TXC	A073	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	ENET_VIO
ENET0_TX_CTL	A071	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	ENET_VIO
ENET_VIO	A059	P	RGMII interface power supply input. This pin must be connected to 1.8V power rail	ENET_VIO

NOTE: RGMII ENET interface must be operated at 1.8V voltage level. 1.8V must be supplied via the ENET_VIO pin if RGMII ENET signals are used for RGMII function on the carrier-board

NOTE: RGMII ENET signals are multifunctional. For additional details please refer to chapter 5 of this document

Table 10 Secondary RGMII ENET1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ENET1_MDC/SAI1_RXD2	B100*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	3.3V/1.8V
ENET1_MDIO/SAI1_RXD3	B099*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	3.3V/1.8V
ENET1_RD0/SAI1_RXD4	A088*	I	Ethernet input data from the PHY	3.3V/1.8V
ENET1_RD1/SAI1_RXD5	A089*	I	Ethernet input data from the PHY	3.3V/1.8V
ENET1_RD2/SAI1_RXD6	A090*	I	Ethernet input data from the PHY	3.3V/1.8V
ENET1_RD3/SAI1_RXD7	A091*	I	Ethernet input data from the PHY	3.3V/1.8V
ENET1_RX_CTL/SAI1_TXFS	A092*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	3.3V/1.8V
ENET1_RXC/SAI1_TXC	A087*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	3.3V/1.8V
ENET1_TD0/SAI1_TXD0	A095*	O	Ethernet output data to PHY	3.3V/1.8V
ENET1_TD1/SAI1_TXD1	A096*	O	Ethernet output data to PHY	3.3V/1.8V
ENET1_TD2/SAI1_TXD2	A097*	O	Ethernet output data to PHY	3.3V/1.8V
ENET1_TD3/SAI1_TXD3	A098*	O	Ethernet output data to PHY	3.3V/1.8V
ENET1_TXC/SAI1_TXD5	A094*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	3.3V/1.8V
ENET1_TX_CTL/SAI1_TXD4	A099*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	3.3V/1.8V

NOTE: RGMII ENET1 interface must be operated at 1.8V voltage level

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.6 PCI-Express

MCM-iMX8M-Plus provides one PCI Express port.

Table 11 PCIE Interface Signals

Signal Name	Pin #	Type	Description
PCIE_REF_CLKN	A020	AO	100 MHz PCIe reference clock differential output negative
PCIE_REF_CLKP	A019	AO	100 MHz PCIe reference clock differential output positive
PCIE_RX_N	A017	I	PCI Express receive data negative
PCIE_RX_P	A018	I	PCI Express receive data positive
PCIE_TX_N	A016	O	PCI Express transmit data negative
PCIE_TX_P	A015	O	PCI Express transmit data positive
PCIE_CLKREQ_B	B015*	O	PCI Express Enable external clock generator

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.7 Sony/Philips Digital Interface (S/PDIF)

MCM-iMX8M-Plus provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX8M Plus Reference manual for additional details. The table below summarizes the S/PDIF interface signals.

Table 12 S/PDIF Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPDIF_EXT_CLK	B055	I	External clock signal	3.3V
	B077			3.3V
SPDIF1_IN	B056	I	SPDIF input data line signal	3.3V
	A109			SD2
	A062			ENET_VIO
	B070			3.3V
SPDIF_TX	B057	O	SPDIF output data line signal	3.3V
	A108			SD2
	A071			ENET_VIO

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.8 Digital Audio (SAI)

MCM-iMX8M-Plus enables access to three of the i.MX8M Plus integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.

- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

Please refer to the i.MX8M Plus Reference manual for additional details.

For SAI signal details please refer to the Signal Multiplexing table in section 5.6.

4.9 USB

i.MX8M Plus SoC is equipped with two dual-role USB3.0 controllers and PHYs.

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the USB3.0 interface signals.

Table 13 USB port #1 Signals

Signal Name	Pin #	Type	Description
USB1_DN	A036	IO	USB2.0 negative data
USB1_DP	A037	IO	USB2.0 positive data
USB1_VBUS_DET	A034	I	USB1 VBUS detect
USB1_TX_N	B020	AO	USB3.0 transmit negative lane
USB1_TX_P	B021	AO	USB3.0 transmit positive lane
USB1_RX_N	A139	AI	USB3.0 receive negative lane
USB1_RX_P	A140	AI	USB3.0 receive positive lane

Table 14 USB port #2 Signals

Signal Name	Pin #	Type	Description
USB2_DN	A039	IO	USB2.0 negative data
USB2_DP	A040	IO	USB2.0 positive data
USB2_VBUS_DET	A038	I	USB2 VBUS detect
USB2_TX_N	A027	AO	USB3.0 transmit negative lane
USB2_TX_P	A028	AO	USB3.0 transmit positive lane
USB2_RX_N	A030	AI	USB3.0 receive negative lane
USB2_RX_P	A031	AI	USB3.0 receive positive lane

4.10 MMC / SD /SDIO

MCM-iMX8M-Plus features two SD/SDIO ports. These ports are derived from the i.MX8M Plus SD/SDIO controllers uSDHC1 and uSDHC2. uSDHC IP supports the following main features:

- Fully compliant with MMC 5.1 command/response sets and physical layer
- Fully compliant with SD 3.01 command/response sets and physical layer

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals.

Table 15 SD/SDIO port #1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
USDHC1_CLK	A049	O	Clock for MMC/SD/SDIO card	3.3V/1.8V
USDHC1_CMD	A047	IO	CMD line connect to card	3.3V/1.8V
USDHC1_DATA0	A054	IO	DATA0 line in all modes. Also used to detect busy state	3.3V/1.8V
USDHC1_DATA1	A051	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	3.3V/1.8V

Signal Name	Pin #	Type	Description	Voltage Domain
USDHC1_DATA2	A050	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	3.3V/1.8V
USDHC1_DATA3	A048	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	3.3V/1.8V
USDHC1_DATA4	A057	IO	DATA4 line in 8-bit mode	3.3V/1.8V
USDHC1_DATA5	A052	IO	DATA5 line in 8-bit mode	3.3V/1.8V
USDHC1_DATA6	A053	IO	DATA6 line in 8-bit mode	3.3V/1.8V
USDHC1_DATA7	A058	IO	DATA7 line in 8-bit mode	3.3V/1.8V
SD1_RESET_B	A055	O	Card hardware reset signal, active LOW	3.3V/1.8V
USDHC1_CD_B	B003	I	Card detect	3.3V
USDHC1_WP	B011	I	Card write protect detection	3.3V

NOTE: SD/SDIO port #1 is pre-configured to operate only at 3.3V voltage levels

NOTE: SDIO pads are multifunctional. For additional details please refer to chapter 5 of this document

Table 16 SD/SDIO port #2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
USDHC2_CD_B	A102	I	Card detection pin	SD2
USDHC2_CLK	A106	O	Clock for MMC/SD/SDIO card	SD2
USDHC2_CMD	A107	IO	CMD line connect to card	SD2
USDHC2_DATA0	A104	IO	DATA0 line in all modes. Also used to detect busy state	SD2
USDHC2_DATA1	A103	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	SD2
USDHC2_DATA2	A108	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	SD2
USDHC2_DATA3	A109	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	SD2
USDHC2_RESET_B	A101	O	Card hardware reset signal, active LOW	SD2
USDHC2_WP	A105	I	Card write protect detection	SD2

NOTE: SD/SDIO port #2 can be configured to operate at 3.3V or 1.8V voltage levels. SD2 voltage domain level is controlled by SoC pin GPIO1_IO04.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

Table 17 SD/SDIO port #3 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
USDHC3_CLK	A063	O	Clock for MMC/SD/SDIO card	ENET_VIO
USDHC3_CMD	A062	IO	CMD line connect to card	ENET_VIO
USDHC3_DATA0	A071	IO	DATA0 line in all modes. Also used to detect busy state	ENET_VIO
USDHC3_DATA1	A073	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	ENET_VIO
USDHC3_DATA2	A065	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	ENET_VIO
USDHC3_DATA3	A064	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	ENET_VIO
USDHC3_DATA4	A067	IO	DATA4 line in 8-bit mode	ENET_VIO
USDHC3_DATA5	A060	IO	DATA5 line in 8-bit mode	ENET_VIO
USDHC3_DATA6	A069	IO	DATA6 line in 8-bit mode	ENET_VIO
USDHC3_DATA7	A072	IO	DATA7 line in 8-bit mode	ENET_VIO
USDHC3_RESET_B	A066	O	Card hardware reset signal, active LOW	ENET_VIO
USDHC3_STROBE	A061	O	MMC strobe	ENET_VIO
USDHC3_WP	A070	I	Card write protect detection	ENET_VIO

NOTE: ENET_VIO must be supplied from carrier-board for proper operation of SDIO #3

NOTE: SDIO pads are multifunctional. For additional details please refer to chapter 5 of this document

4.11 UART

MCM-iMX8M-Plus enables access to up-to four i.MX8M Plus universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The i.MX8M Plus UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: By default UART2 is assigned to be used as the main system console port.

NOTE: By default UART4 is assigned to be used as the M7 core debug port.

Please refer to the i.MX8M Plus Reference manual for additional details.

For UART signal details please refer to the Signal Multiplexing table in section 5.6.

4.12 CAN Bus

MCM-iMX8M-Plus features up-to two CAN bus interfaces. These interfaces support the following key features:

- Full implementation of the CAN version 2.0B
- Compliant with the ISO 11898-1 standard

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the CAN interface signals.

Table 18 CAN1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN1_TX	B082*	O	CAN transmit pin	3.3V
	B057*			3.3V
	B052*			3.3V
CAN1_RX	B083*	I	CAN receive pin	3.3V
	B056*			3.3V
	B053*			3.3V

Table 19 CAN2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN2_TX	B112*	O	CAN transmit pin	3.3V
	B079*			3.3V
	B061*			3.3V
CAN2_RX	B080*	I	CAN receive pin	3.3V
	B111*			3.3V
	B095*			3.3V/1.8V
	B060*			3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.13 I2C

MCM-iMX8M-Plus features up-to five I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode

Please refer to the i.MX8M Plus Reference manual for additional details.

NOTE: I2C2 is the system I2C channel utilized for the following on-board functions: RTC, EEPROM.

For I2C signal details please refer to the Signal Multiplexing table in section 5.6.

4.14 ECSPI

Up-to two SPI interfaces are accessible through the MCM-iMX8M-Plus carrier board interface. The SPI interfaces are derived from i.MX8M Plus integrated synchronous serial interface (eCSPI). Each instance of the eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s
- Full-duplex synchronous serial interface
- Master/Slave configurable
- One Chip Select (SS) signal
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the ECSPI interface signals.

Table 20 ECSPI2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ECSPI2_MISO	B064*	I	SPI-2 Master data in; slave data out	3.3V
	B015*			3.3V
	A109*			SD2
ECSPI2_MOSI	B114*	O	SPI-2 Master data out; slave data in	3.3V
	B063*			3.3V
	A107*			SD2
ECSPI2_SCLK	B115*	O	SPI-2 Master clock out; slave clock in	3.3V
	B065*			3.3V
	A106*			SD2
ECSPI2_SS0	B062*	O	SPI-2 Chip select 0	3.3V
	A108*			SD2

Table 21 ECSPI3 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ECSPI3_MISO	A112*	I	SPI-3 Master data in; slave data out	3.3V
ECSPI3_MOSI	B086*	O	SPI-3 Master data out; slave data in	3.3V
ECSPI3_SCLK	B085*	O	SPI-3 Master clock out; slave clock in	3.3V
ECSPI3_SS0	A113*	O	SPI-3 Chip select 0	3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.15 PWM

MCM-iMX8M-Plus features up to four independent PWM output signals. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the PWM interface signals.

Table 22 PWM Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
PWM1_OUT	B055*	O	PWM1 functional output	3.3V
	B095*			3.3V/1.8V
	B012*			3.3V
PWM2_OUT	B056*	O	PWM2 functional output	3.3V
	B094*			3.3V/1.8V
	B015*			3.3V
PWM3_OUT	B057*	O	PWM3 functional output	3.3V
	B096*			3.3V/1.8V
	B114*			3.3V
PWM4_OUT	B069*	O	PWM4 functional output	3.3V
	B097*			3.3V/1.8V
	B115*			3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.16 JTAG

MCM-iMX8M-Plus enables access to the i.MX8M Plus JTAG port through the carrier board interface.

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the JTAG interface signals.

Table 23 JTAG Interface Signals

Signal Name	Pin #	Type	Description
JTAG_MOD	A042	I	JTAG MODE
JTAG_TCK	A043	I	Test Clock
JTAG_TDI	A045	I	Test Data In
JTAG_TDO	A044	O	Test Data Out
JTAG_TMS	A046	I	Test Mode Select

4.17 GPIO

Up-to 115 of the i.MX8M Plus general purpose input/output (GPIO) signals are available through the MCM-iMX8M-Plus carrier board interface. When configured as an output, it is possible to write to an i.MX8M Plus register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M Plus register. In addition, GPIO signals can produce interrupts.
Please refer to the i.MX8M Plus Reference manual for additional details.
The table below summarizes the GPIO interface signals.

Table 24 GPIO Signals

Signal Name	Pin #	Type	Description	Voltage Domain
GPIO1_IO0	B009*	IO	GPIO	3.3V
GPIO1_IO1	B012*	IO	GPIO	3.3V
GPIO1_IO18	A069*	IO	GPIO	ENET_VIO
GPIO1_IO19	A072*	IO	GPIO	ENET_VIO
GPIO1_IO20	A068*	IO	GPIO	ENET_VIO
GPIO1_IO21	A070*	IO	GPIO	ENET_VIO
GPIO1_IO22	A071*	IO	GPIO	ENET_VIO
GPIO1_IO23	A073*	IO	GPIO	ENET_VIO
GPIO1_IO24	A065*	IO	GPIO	ENET_VIO
GPIO1_IO25	A064*	IO	GPIO	ENET_VIO
GPIO1_IO26	A067*	IO	GPIO	ENET_VIO
GPIO1_IO27	A066*	IO	GPIO	ENET_VIO
GPIO1_IO28	A063*	IO	GPIO	ENET_VIO
GPIO1_IO29	A062*	IO	GPIO	ENET_VIO
GPIO2_IO0	A049*	IO	GPIO	3.3V/1.8V
GPIO2_IO1	A047*	IO	GPIO	3.3V/1.8V
GPIO2_IO10	A055*	IO	GPIO	3.3V/1.8V
GPIO2_IO12	A102*	O	GPIO	SD2
GPIO2_IO13	A106*	O	GPIO	SD2
GPIO2_IO14	A107*	IO	GPIO	SD2
GPIO2_IO15	A104*	IO	GPIO	SD2
GPIO2_IO16	A103*	IO	GPIO	SD2
GPIO2_IO17	A108*	IO	GPIO	SD2
GPIO2_IO18	A109*	IO	GPIO	SD2
GPIO2_IO19	A101*	IO	GPIO	SD2
GPIO2_IO2	A054*	IO	GPIO	3.3V/1.8V
GPIO2_IO20	A105*	IO	GPIO	SD2
GPIO2_IO3	A051*	IO	GPIO	3.3V/1.8V
GPIO2_IO4	A050*	IO	GPIO	3.3V/1.8V
GPIO2_IO5	A048*	IO	GPIO	3.3V/1.8V
GPIO3_IO19	B097*	IO	GPIO	3.3V/1.8V
GPIO3_IO20	B096*	IO	GPIO	3.3V/1.8V
GPIO3_IO21	B094*	IO	GPIO	3.3V/1.8V
GPIO3_IO25	B095*	IO	GPIO	3.3V/1.8V
GPIO3_IO26	B052*	IO	GPIO	3.3V
GPIO3_IO27	B053*	IO	GPIO	3.3V
GPIO3_IO28	B061*	IO	GPIO	3.3V
GPIO3_IO29	B060*	IO	GPIO	3.3V
GPIO4_IO10	A092*	IO	GPIO	3.3V/1.8V
GPIO4_IO11	A087*	IO	GPIO	3.3V/1.8V

Signal Name	Pin #	Type	Description	Voltage Domain
GPIO4_IO12	A095*	IO	GPIO	3.3V/1.8V
GPIO4_IO14	A097*	IO	GPIO	3.3V/1.8V
GPIO4_IO15	A098*	IO	GPIO	3.3V/1.8V
GPIO4_IO16	A099*	IO	GPIO	3.3V/1.8V
GPIO4_IO17	A094*	IO	GPIO	3.3V/1.8V
GPIO4_IO19	B107*	IO	GPIO	3.3V/1.8V
GPIO4_IO20	B047*	IO	GPIO	3.3V/1.8V
GPIO4_IO21	B109*	IO	GPIO	3.3V
GPIO4_IO22	B082*	IO	GPIO	3.3V
GPIO4_IO24	B110*	IO	GPIO	3.3V
GPIO4_IO25	B083*	IO	GPIO	3.3V
GPIO4_IO26	B079*	IO	GPIO	3.3V
GPIO4_IO27	B080*	IO	GPIO	3.3V
GPIO4_IO28	B070*	IO	GPIO	3.3V
GPIO4_IO29	B072*	IO	GPIO	3.3V
GPIO4_IO30	B073*	IO	GPIO	3.3V
GPIO4_IO31	B074*	IO	GPIO	3.3V
GPIO4_IO8	A090*	IO	GPIO	3.3V/1.8V
GPIO4_IO9	A091*	IO	GPIO	3.3V/1.8V
GPIO5_IO0	B076*	IO	GPIO	3.3V
GPIO5_IO1	B077*	IO	GPIO	3.3V
GPIO5_IO10	B065*	IO	GPIO	3.3V
GPIO5_IO11	B063*	IO	GPIO	3.3V
GPIO5_IO12	B064*	IO	GPIO	3.3V
GPIO5_IO13	B062*	IO	GPIO	3.3V
GPIO5_IO18	B115*	IO	GPIO	3.3V
GPIO5_IO19	B114*	IO	GPIO	3.3V
GPIO5_IO2	B069*	IO	GPIO	3.3V
GPIO5_IO20	B015*	IO	GPIO	3.3V
GPIO5_IO22	B085*	IO	GPIO	3.3V
GPIO5_IO23	B086*	IO	GPIO	3.3V
GPIO5_IO24	A112*	IO	GPIO	3.3V
GPIO5_IO25	A113*	IO	GPIO	3.3V
GPIO5_IO26	B112*	IO	GPIO	3.3V
GPIO5_IO27	B111*	IO	GPIO	3.3V
GPIO5_IO28	A110*	IO	GPIO	3.3V
GPIO5_IO29	A111*	IO	GPIO	3.3V
GPIO5_IO3	B057*	IO	GPIO	3.3V
GPIO5_IO4	B056*	IO	GPIO	3.3V
GPIO5_IO5	B055*	IO	GPIO	3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE: GPIOs that belong to the ENET_VIO power domain can operate at 1.8V or 2.5V or 3.3V voltage levels. Required voltage must be supplied via the ENET_VIO pin if any of these signals are used as GPIOs on the carrier-board

5 SYSTEM LOGIC

5.1 Power Supply

Table 25 Power signals

Signal Name	Pin#	Type	Description
V_SOM	A021, A032 B018	P	Main power supply. Connect to a regulated DC supply or Li-Ion battery
VCC_RTC	A023	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. If RTC back-up is not required, connect this pin to GND.
GND	A005, A008, A014, A026, A029, A041, A056, A074, A077, A080, A083, A086, A093, A118, A121, A130, A133, A138 B001, B008, B013, B016, B022, B029, B030, B033, B036, B039, B042, B045, B050, B054, B058, B059, B066, B071, B075, B078, B081, B084, B087, B088, B093, B098, B103, B106, B113, B116	P	Common ground
ENET_VIO	A059	P	RGMII0 interface power supply input. This pin must be connected to 1.8V or 3.3V power rail depending on the PHY requirements

5.2 I/O Voltage Domains

MCM-iMX8M-Plus utilizes four separate I/O voltage domains to power different I/O modules of the i.MX8M Plus SoC:

Table 26 Power signals

I/O Voltage Domain	Description	Default Voltage	Control
3.3V domain	Main SoM 3.3V	3.3V	N/A
ENET_VIO domain	RGMII0 interface power supply. This domain must be supplied from carrier-board via pin ENET_VIO.	ENET_VIO	N/A
SD2 domain	SD interface power supply. Powered with PMIC LDO5.	3.3V	SoC pin GPIO1_IO04
3.3V/1.8V domain	Software programmable 3.3V/1.8V voltage rail. Powered with PMIC LDO4.	1.8V	Configuring LDO4 in u-boot

5.3 System and Miscellaneous Signals

5.3.1 External regulator control and power management

MCM-iMX8M-Plus supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX8M Plus SoC. The logic that controls both signals is supplied by the i.MX8M Plus SoC SNVS power rail.

The PMIC_STBY_REQ output can be used to signal the carrier board power supply that MCM-iMX8M-Plus is in 'standby' or 'OFF' mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX8M Plus Reference manual for additional details. The table below summarizes the external regulator control signals.

Table 27 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY_REQ	A013	O	When the processor enters SUSPEND mode, it will assert this signal.	Always available
PMIC_ON_REQ	B046	O	Active high power-up request output from i.MX8M Plus SoC.	Always available
PWRBTN	A033	I	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).	Always available

5.4 Reset

SYS_RST_PMIC signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on MCM-iMX8M-Plus. Please refer to the i.MX8M Plus Reference manual for additional details.

Table 28 Reset signals

Signal Name	Pin #	Type	Description	Availability
SYS_RST_PMIC	A022	I	Active Low cold reset input signal. Should be used as main system reset	Always available

5.5 Boot Sequence

MCM-iMX8M-Plus boot sequence defines which interface/media is used by MCM-iMX8M-Plus to load and execute the initial software (such as SPL or/and U-boot). MCM-iMX8M-Plus can load initial software from the following interfaces/media:

- The on-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD card using the SD/SDIO 2 interface

MCM-iMX8M-Plus will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by MCM-iMX8M-Plus:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: designed to allow recovery from an external boot device in case of data corruption of the on-board primary boot device. Using the alternate sequence allows MCM-iMX8M-Plus to boot from an external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 29 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	A100	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence	Always available

Table 30 MCM-iMX8M-Plus Boot sequences

Sequence	ALT_BOOT	First
Standard	Low or floating	Onboard eMMC (primary boot storage)
Alternate	High	SD card on SD/SDIO2 interface

5.6 Signal Multiplexing Characteristics

Up to 119 of the MCM-iMX8M-Plus pads are multifunctional. Multifunctional pads enable extensive functional flexibility of the MCM-iMX8M-Plus CoM/SoM by allowing usage of a single pad for one of several functions. Up-to 6 functions (MUX modes) are accessible through each multifunctional pad. The multifunctional capabilities of MCM-iMX8M-Plus pads are derived from the i.MX8M Plus SoC control module

NOTE: Pad function selection is controlled by software.

NOTE: Each pad can be used for a single function at a time.

NOTE: Only one pad can be used for each function (in case a function is available on more than one pad).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 31 Multifunctional Signals

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
B091	ECSPI1_MISO	3.3V	GPIO5_IO8	SAI7_RX_DATA0		I2C2_SCL	UART3_CTS_B			ECSPI1_MISO					
B092	ECSPI1_MOSI	3.3V	GPIO5_IO7	SAI7_RX_BCLK		I2C1_SDA	UART3_TX			ECSPI1_MOSI					
B089	ECSPI1_SCLK	3.3V	GPIO5_IO6	SAI7_RX_SYNC		I2C1_SCL	UART3_RX			ECSPI1_SCLK					
B090	ECSPI1_SS0	3.3V	GPIO5_IO9	SAI7_TX_SYNC		I2C2_SDA	UART3_RTS_B			ECSPI1_SS0					
B064	ECSPI2_MISO	3.3V	GPIO5_IO12	SAI7_MCLK		I2C4_SCL	UART4_CTS_B			ECSPI2_MISO					
B063	ECSPI2_MOSI	3.3V	GPIO5_IO11	SAI7_TX_DATA0		I2C3_SDA	UART4_TX			ECSPI2_MOSI					
B065	ECSPI2_SCLK	3.3V	GPIO5_IO10	SAI7_TX_BCLK		I2C3_SCL	UART4_RX			ECSPI2_SCLK					
B062	ECSPI2_SS0	3.3V	GPIO5_IO13			I2C4_SDA	UART4_RTS_B			ECSPI2_SS0					
A061	ENET_MDC	ENET_VIO	GPIO1_IO16	SAI6_TX_DATA0	USDHC3_STROBE				ENET_QOS_MDC						
A060	ENET_MDIO	ENET_VIO	GPIO1_IO17	SAI6_TX_SYNC	USDHC3_DATA5				ENET_QOS_MDIO						
A067	ENET_RD0	ENET_VIO	GPIO1_IO26	SAI7_RX_DATA0	USDHC3_DATA4				ENET_QOS_RD0						
A066	ENET_RD1	ENET_VIO	GPIO1_IO27	SAI7_RX_SYNC	USDHC3_RESET_B				ENET_QOS_RD1						
A063	ENET_RD2	ENET_VIO	GPIO1_IO28	SAI7_RX_BCLK	USDHC3_CLK				ENET_QOS_RD2						
A062	ENET_RD3	ENET_VIO	GPIO1_IO29	SAI7_MCLK	USDHC3_CMD				ENET_QOS_RD3						SPDIF1_IN

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
A065	ENET_RX_CTL	ENET_VIO	GPIO1_IO24	SAI7_TX_SYNC	USDHC3_DATA2				ENET_QOS_RX_CTL						
A064	ENET_RXC	ENET_VIO	GPIO1_IO25	SAI7_TX_BCLK	USDHC3_DATA3				ENET_QOS_RXC ENET_QOS_RX_ER						
A070	ENET_TD0	ENET_VIO	GPIO1_IO21	SAI6_RX_BCLK	USDHC3_WP				ENET_QOS_TD0						
A068	ENET_TD1	ENET_VIO	GPIO1_IO20	SAI6_RX_SYNC	USDHC3_CD_B				ENET_QOS_TD1						
A072	ENET_TD2	ENET_VIO	GPIO1_IO19	SAI6_RX_DATA0	USDHC3_DATA7				ENET_QOS_TD2 ENET_QOS_TX_CLK						
A069	ENET_TD3	ENET_VIO	GPIO1_IO18	SAI6_TX_BCLK	USDHC3_DATA6				ENET_QOS_TD3						
A071	ENET_TX_CTL	ENET_VIO	GPIO1_IO22	SAI6_MCLK	USDHC3_DATA0				ENET_QOS_TX_CTL						SPDIF1_OUT
A073	ENET_TXC	ENET_VIO	GPIO1_IO23	SAI7_TX_DATA0	USDHC3_DATA1				ENET_QOS_TXC ENET_QOS_TX_ER						
B009	GPIO1_IO00	3.3V	GPIO1_IO0												
B012	GPIO1_IO01	3.3V	GPIO1_IO1								PWM1_OUT				
B004	GPIO1_IO05	3.3V	GPIO1_IO5												
B003	GPIO1_IO06	3.3V	GPIO1_IO6		USDHC1_CD_B				ENET_QOS_MDC						
B011	GPIO1_IO07	3.3V	GPIO1_IO7		USDHC1_WP				ENET_QOS_MDIO						
B010	GPIO1_IO08	3.3V	GPIO1_IO8		USDHC2_RESET_B				ENET_QOS_1588_EVENT0_IN ENET_QOS_1588_EVENT0_AUX_IN		PWM1_OUT				
B067	GPIO1_IO10	3.3V	GPIO1_IO10								PWM3_OUT				
B017	GPIO1_IO11	3.3V	GPIO1_IO11		USDHC3_VSELECT						PWM2_OUT				
B006	GPIO1_IO13	3.3V	GPIO1_IO13								PWM2_OUT				
B007	GPIO1_IO15	3.3V	GPIO1_IO15		USDHC3_WP						PWM4_OUT				
B061	HDMI_CEC	3.3V	GPIO3_IO28			I2C6_SCL						CAN2_TX		HDMI_CEC	
B052	HDMI_DDC_SCL	3.3V	GPIO3_IO26			I2C5_SCL						CAN1_TX		HDMI_SCL	
B053	HDMI_DDC_SDA	3.3V	GPIO3_IO27			I2C5_SDA						CAN1_RX		HDMI_SDA	
B060	HDMI_HPD	3.3V	GPIO3_IO29			I2C6_SDA						CAN2_RX		HDMI_HPD	
B115	I2C3_SCL	3.3V	GPIO5_IO18			I2C3_SCL				ECSPI2_SCLK	PWM4_OUT				
B114	I2C3_SDA	3.3V	GPIO5_IO19			I2C3_SDA				ECSPI2_MOSI	PWM3_OUT				
B015	I2C4_SCL	3.3V	GPIO5_IO20			I2C4_SCL				ECSPI2_MISO	PWM2_OUT				
B014	I2C4_SDA	3.3V	GPIO5_IO21			I2C4_SDA				ECSPI2_SS0	PWM1_OUT				

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
B023	NAND_ALE	1.8V	GPIO3_IO0	SAI3_TX_BCLK			UART3_RX						QSPI_SCLK		
B024	NAND_CE0_B	1.8V	GPIO3_IO1	SAI3_TX_DATA0			UART3_TX						QSPI_SS0_B		
B028	NAND_DATA00	1.8V	GPIO3_IO6	SAI3_RX_DATA0			UART4_RX						QSPI_DATA0		
B027	NAND_DATA01	1.8V	GPIO3_IO7	SAI3_TX_SYNC			UART4_TX						QSPI_DATA1		
B026	NAND_DATA02	1.8V	GPIO3_IO8		USDHC3_CD_B	I2C4_SDA	UART4_CTS_B						QSPI_DATA2		
B025	NAND_DATA03	1.8V	GPIO3_IO9		USDHC3_WP		UART4_RTS_B						QSPI_DATA3		
B047	SAI1_MCLK	3V3/1V8	GPIO4_IO20	SAI1_MCLK SAI1_TX_BCLK				ENET1_TX_CLK							
B104	SAI1_RXC	3V3/1V8	GPIO4_IO1	SAI1_RX_BCLK				ENET1_1588_EVENT0_OUT							
B102	SAI1_RXD0	3V3/1V8	GPIO4_IO2	SAI1_RX_DATA0 SAI1_TX_DATA1				ENET1_1588_EVENT1_IN							
B101	SAI1_RXD1	3V3/1V8	GPIO4_IO3	SAI1_RX_DATA1				ENET1_1588_EVENT1_OUT							
B100	SAI1_RXD2	3V3/1V8	GPIO4_IO4	SAI1_RX_DATA2				ENET1_MDC							
B099	SAI1_RXD3	3V3/1V8	GPIO4_IO5	SAI1_RX_DATA3				ENET1_MDIO							
A088	SAI1_RXD4	3V3/1V8	GPIO4_IO6	SAI1_RX_DATA4 SAI6_TX_BCLK SAI6_RX_BCLK				ENET1_RD0							
A089	SAI1_RXD5	3V3/1V8	GPIO4_IO7	SAI1_RX_DATA5/SAI6_TX_DATA0/SAI6_RX_DATA0/SAI1_RX_SYNC				ENET1_RD1							
A090	SAI1_RXD6	3V3/1V8	GPIO4_IO8	SAI1_RX_DATA6/SAI6_TX_SYNC/SAI6_RX_SYNC				ENET1_RD2							
A091	SAI1_RXD7	3V3/1V8	GPIO4_IO9	SAI1_RX_DATA7 SAI6_MCLK SAI1_TX_SYNC SAI1_TX_DATA4				ENET1_RD3							
B105	SAI1_RXFS	3V3/1V8	GPIO4_IO0	SAI1_RX_SYNC				ENET1_1588_EVENT0_IN							
A087	SAI1_TXC	3V3/1V8	GPIO4_IO11	SAI1_TX_BCLK				ENET1_RXC							
A095	SAI1_TXD0	3V3/1V8	GPIO4_IO12	SAI1_TX_DATA0				ENET1_TD0							
A096	SAI1_TXD1	3V3/1V8	GPIO4_IO13	SAI1_TX_DATA1				ENET1_TD1							
A097	SAI1_TXD2	3V3/1V8	GPIO4_IO14	SAI1_TX_DATA2				ENET1_TD2							
A098	SAI1_TXD3	3V3/1V8	GPIO4_IO15	SAI1_TX_DATA3				ENET1_TD3							
A099	SAI1_TXD4	3V3/1V8	GPIO4_IO16	SAI1_TX_DATA4 SAI6_RX_BCLK				ENET1_TX_CTL							

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
				SAI6_TX_BCLK											
A094	SAI1_TXD5	3V3/1V8	GPIO4_IO17	SAI1_TX_DATA5 SAI6_RX_DATA0 SAI6_TX_DATA0				ENET1_TXC							
B108	SAI1_TXD6	3V3/1V8	GPIO4_IO18	SAI1_TX_DATA6 SAI6_RX_SYNC SAI6_TX_SYNC				ENET1_RX_ER							
B107	SAI1_TXD7	3V3/1V8	GPIO4_IO19	SAI1_TX_DATA7 SAI6_MCLK				ENET1_TX_ER							
A092	SAI1_TXFS	3V3/1V8	GPIO4_IO10	SAI1_TX_SYNC				ENET1_RX_CTL							
B080	SAI2_MCLK	3.3V	GPIO4_IO27	SAI2_MCLK SAI5_MCLK SAI3_MCLK								CAN2_RX			
B082	SAI2_RXC	3.3V	GPIO4_IO22	SAI2_RX_BCLK SAI5_TX_BCLK			UART1_RX					CAN1_TX			
B068	SAI2_RXD0	3.3V	GPIO4_IO23	SAI2_RX_DATA0 SAI5_TX_DATA0 SAI2_TX_DATA1			UART1_RTS_B		ENET_QOS_1588_EVENT2_OUT						
B109	SAI2_RXFS	3.3V	GPIO4_IO21	SAI2_RX_SYNC SAI5_TX_SYNC SAI5_TX_DATA1 SAI2_RX_DATA1			UART1_TX								
B083	SAI2_TXC	3.3V	GPIO4_IO25	SAI2_TX_BCLK SAI5_TX_DATA2								CAN1_RX			
B079	SAI2_TXD0	3.3V	GPIO4_IO26	SAI2_TX_DATA0 SAI5_TX_DATA3								CAN2_TX			
B110	SAI2_TXFS	3.3V	GPIO4_IO24	SAI2_TX_SYNC SAI5_TX_DATA1 SAI2_TX_DATA1			UART1_CTS_B		ENET_QOS_1588_EVENT3_OUT						
B069	SAI3_MCLK	3.3V	GPIO5_IO2	SAI3_MCLK SAI5_MCLK							PWM4_OUT				SPDIF1_OUT/SPDIF1_IN
B072	SAI3_RXC	3.3V	GPIO4_IO29	SAI3_RX_BCLK SAI2_RX_DATA2 SAI5_RX_BCLK			UART2_CTS_B								
B073	SAI3_RXD	3.3V	GPIO4_IO30	SAI3_RX_DATA0 SAI2_RX_DATA3 SAI5_RX_DATA0			UART2_RTS_B								
B070	SAI3_RXFS	3.3V	GPIO4_IO28	SAI3_RX_SYNC SAI2_RX_DATA1 SAI5_RX_SYNC SAI3_RX_DATA1											SPDIF1_IN
B076	SAI3_TXC	3.3V	GPIO5_IO0	SAI3_TX_BCLK SAI2_TX_DATA2 SAI5_RX_DATA2			UART2_TX								
B077	SAI3_TXD	3.3V	GPIO5_IO1	SAI3_TX_DATA0 SAI2_TX_DATA3 SAI5_RX_DATA3											SPDIF1_EXT_CLK
B074	SAI3_TXFS	3.3V	GPIO4_IO31	SAI3_TX_SYNC			UART2_RX								

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
				SAI2_TX_DATA1 SAI5_RX_DATA1 SAI3_TX_DATA1											
B095	SAI5_MCLK	3V3/1V8	GPIO3_IO25	SAI5_MCLK SAI1_TX_BCLK		I2C5_SDA					PWM1_OUT	CAN2_RX			
B096	SAI5_RXC	3V3/1V8	GPIO3_IO20	SAI5_RX_BCLK SAI1_TX_DATA1		I2C6_SDA					PWM3_OUT				
B094	SAI5_RXD0	3V3/1V8	GPIO3_IO21	SAI5_RX_DATA0 SAI1_TX_DATA2		I2C5_SCL					PWM2_OUT				
A035	SAI5_RXD1	3V3/1V8	GPIO3_IO22	SAI5_RX_DATA1 SAI1_TX_DATA3 SAI1_TX_SYNC SAI5_TX_SYNC								CAN1_TX			
B019	SAI5_RXD2	3V3/1V8	GPIO3_IO23	SAI5_RX_DATA2 SAI1_TX_DATA4 SAI1_TX_SYNC SAI5_TX_BCLK								CAN1_RX			
B005	SAI5_RXD3	3V3/1V8	GPIO3_IO24	SAI5_RX_DATA3 SAI1_TX_DATA5 SAI1_TX_SYNC SAI5_TX_DATA0								CAN2_TX			
B097	SAI5_RXFS	3V3/1V8	GPIO3_IO19	SAI5_RX_SYNC SAI1_TX_DATA0		I2C6_SCL					PWM4_OUT				
A049	SD1_CLK	3V3/1V8	GPIO2_IO0		USDHC1_CLK	I2C5_SCL	UART1_TX	ENET1_MDC							
A047	SD1_CMD	3V3/1V8	GPIO2_IO1		USDHC1_CMD	I2C5_SDA	UART1_RX	ENET1_MDIO							
A054	SD1_DATA0	3V3/1V8	GPIO2_IO2		USDHC1_DATA0	I2C6_SCL	UART1_RTS_B	ENET1_TD1							
A051	SD1_DATA1	3V3/1V8	GPIO2_IO3		USDHC1_DATA1	I2C6_SDA	UART1_CTS_B	ENET1_TD0							
A050	SD1_DATA2	3V3/1V8	GPIO2_IO4		USDHC1_DATA2	I2C4_SCL	UART2_TX	ENET1_RD0							
A048	SD1_DATA3	3V3/1V8	GPIO2_IO5		USDHC1_DATA3	I2C4_SDA	UART2_RX	ENET1_RD1							
A057	SD1_DATA4	3V3/1V8	GPIO2_IO6		USDHC1_DATA4	I2C1_SCL	UART2_RTS_B	ENET1_TX_CTL							
A052	SD1_DATA5	3V3/1V8	GPIO2_IO7		USDHC1_DATA5	I2C1_SDA	UART2_CTS_B	ENET1_TX_ER							
A053	SD1_DATA6	3V3/1V8	GPIO2_IO8		USDHC1_DATA6	I2C2_SCL	UART3_TX	ENET1_RX_CTL							
A058	SD1_DATA7	3V3/1V8	GPIO2_IO9		USDHC1_DATA7	I2C2_SDA	UART3_RX	ENET1_RX_ER							
A055	SD1_RESET_B	3V3/1V8	GPIO2_IO10		USDHC1_RESET_B	I2C3_SCL	UART3_RTS_B	ENET1_TX_CLK							
A102	SD2_CD_B	SD2	GPIO2_IO12		USDHC2_CD_B										
A106	SD2_CLK	SD2	GPIO2_IO13		USDHC2_CLK		UART4_RX			ECSPI2_SCLK					
A107	SD2_CMD	SD2	GPIO2_IO14		USDHC2_CMD		UART4_TX			ECSPI2_MOSI					

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
A104	SD2_DATA0	SD2	GPIO2_IO15		USDHC2_DATA0	I2C4_SDA	UART2_RX								
A103	SD2_DATA1	SD2	GPIO2_IO16		USDHC2_DATA1	I2C4_SCL	UART2_TX								
A108	SD2_DATA2	SD2	GPIO2_IO17		USDHC2_DATA2					ECSPI2_SS0					SPDIF1_OUT
A109	SD2_DATA3	SD2	GPIO2_IO18		USDHC2_DATA3					ECSPI2_MISO					SPDIF1_IN
A101	SD2_RESET_B	SD2	GPIO2_IO19		USDHC2_RESET_B										
A105	SD2_WP	SD2	GPIO2_IO20		USDHC2_WP										
B055	SPDIF_EXT_CLK	3.3V	GPIO5_IO5								PWM1_OUT				SPDIF1_EXT_CLK
B056	SPDIF_RX	3.3V	GPIO5_IO4			I2C5_SDA					PWM2_OUT	CAN1_RX			SPDIF1_IN
B057	SPDIF_TX	3.3V	GPIO5_IO3			I2C5_SCL					PWM3_OUT	CAN1_TX			SPDIF1_OUT
B085	UART1_RXD	3.3V	GPIO5_IO22				UART1_RX			ECSPI3_SCLK					
B086	UART1_TXD	3.3V	GPIO5_IO23				UART1_TX			ECSPI3_MOSI					
A112	UART2_RXD	3.3V	GPIO5_IO24				UART2_RX			ECSPI3_MISO					
A113	UART2_TXD	3.3V	GPIO5_IO25				UART2_TX			ECSPI3_SS0					
B112	UART3_RXD	3.3V	GPIO5_IO26		USDHC3_RESET_B		UART3_RX UART1_CTS_B					CAN2_TX			
B111	UART3_TXD	3.3V	GPIO5_IO27		USDHC3_VSELECT		UART3_TX UART1_RTS_B					CAN2_RX			
A110	UART4_RXD	3.3V	GPIO5_IO28			I2C6_SCL	UART4_RX UART2_CTS_B								
A111	UART4_TXD	3.3V	GPIO5_IO29			I2C6_SDA	UART4_TX UART2_RTS_B								

5.7 RTC

MCM-iMX8M-Plus features an on-board ultra-low-power AM1805 real time clock (RTC). The RTC is connected to the i.MX8M SoC using I2C2 interface at address 0xD2/D3.

Back-up power supply is required in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about MCM-iMX8M-Plus RTC please refer to the AM1805 datasheet.

5.8 LED

MCM-iMX8M-Plus features a single general purpose green LED controlled by GPIO1_IO[12] signal of the i.MX8M Plus. The LED is ON when GPIO1_IO[12] is logic LOW.

5.9 Reserved Signals

The following MCM-iMX8M-Plus signals are reserved and must be left unconnected.

Table 32 Reserved Signals

Signal Name	Pin#
RESERVED1	A055

6 CARRIER BOARD INTERFACE

The MCM-iMX8M-Plus SoM carrier board interface uses 256-pin QFN package. The SoM pinout is detailed in the table below.

6.1 Package Pinout

Table 33 External Pads

Pad #	MCM-iMX8M-Plus Signal Name		Pad #	MCM-iMX8M-Plus Signal Name
A001	MIPI_CSI1_D3_N		A071	ENET_TX_CTL
A002	MIPI_CSI1_D3_P		A072	ENET_TD2
A003	MIPI_CSI1_D2_N		A073	ENET_TXC
A004	MIPI_CSI1_D2_P		A074	GND
A005	GND		A075	HDMI_TX2N
A006	MIPI_CSI1_CLK_N		A076	HDMI_TX2P
A007	MIPI_CSI1_CLK_P		A077	GND
A008	GND		A078	HDMI_TX1N
A009	MIPI_CSI1_D1_N		A079	HDMI_TX1P
A010	MIPI_CSI1_D1_P		A080	GND
A011	MIPI_CSI1_D0_N		A081	HDMI_TX0N
A012	MIPI_CSI1_D0_P		A082	HDMI_TX0P
A013	PMIC_STBY_REQ		A083	GND
A014	GND		A084	HDMI_TXCN
A015	PCIE_TX_P		A085	HDMI_TXCP
A016	PCIE_TX_N		A086	GND
A017	PCIE_RX_N		A087	SAI1_TXC
A018	PCIE_RX_P		A088	SAI1_RXD4
A019	PCIE_REF_CLKP		A089	SAI1_RXD5
A020	PCIE_REF_CLKN		A090	SAI1_RXD6
A021	V_SOM		A091	SAI1_RXD7
A022	SYS_RST_PMIC		A092	SAI1_TXFS
A023	VCC_RTC		A093	GND
A024	SYS_I2C_SDA		A094	SAI1_TXD5
A025	SYS_I2C_SCL		A095	SAI1_TXD0
A026	GND		A096	SAI1_TXD1
A027	USB2_TX_N		A097	SAI1_TXD2
A028	USB2_TX_P		A098	SAI1_TXD3
A029	GND		A099	SAI1_TXD4
A030	USB2_RX_N		A100	ALT_BOOT
A031	USB2_RX_P		A101	SD2_RESET_B
A032	V_SOM		A102	SD2_NCD
A033	PWRBTN		A103	SD2_DATA1
A034	USB1_VBUS		A104	SD2_DATA0
A035	SAI5_RXD1		A105	SD2_WP
A036	USB1_DN		A106	SD2_CLK
A037	USB1_DP		A107	SD2_CMD
A038	USB2_VBUS		A108	SD2_DATA2

A039	USB2_DN		A109	SD2_DATA3
A040	USB2_DP		A110	UART4_RXD
A041	GND		A111	UART4_TXD
A042	JTAG_MOD		A112	UART2_RXD
A043	JTAG_TCK		A113	UART2_TXD
A044	JTAG_TDO		A114	MIPI_DSI1_D0_N
A045	JTAG_TDI		A115	MIPI_DSI1_D0_P
A046	JTAG_TMS		A116	MIPI_DSI1_D1_N
A047	SD1_CMD		A117	MIPI_DSI1_D1_P
A048	SD1_DATA3		A118	GND
A049	SD1_CLK		A119	MIPI_DSI1_CLK_N
A050	SD1_DATA2		A120	MIPI_DSI1_CLK_P
A051	SD1_DATA1		A121	GND
A052	SD1_DATA5		A122	MIPI_DSI1_D2_N
A053	SD1_DATA6		A123	MIPI_DSI1_D2_P
A054	SD1_DATA0		A124	MIPI_DSI1_D3_N
A055	CLAB_RESERVED1		A125	MIPI_DSI1_D3_P
A056	GND		A126	MIPI_CSI2_D3_N
A057	SD1_DATA4		A127	MIPI_CSI2_D3_P
A058	SD1_DATA7		A128	MIPI_CSI2_D2_N
A059	ENET_VIO		A129	MIPI_CSI2_D2_P
A060	ENET_MDIO		A130	GND
A061	ENET_MDC		A131	MIPI_CSI2_CLK_N
A062	ENET_RD3		A132	MIPI_CSI2_CLK_P
A063	ENET_RD2		A133	GND
A064	ENET_RXC		A134	MIPI_CSI2_D1_N
A065	ENET_RX_CTL		A135	MIPI_CSI2_D1_P
A066	ENET_RD1		A136	MIPI_CSI2_D0_N
A067	ENET_RD0		A137	MIPI_CSI2_D0_P
A068	ENET_TD1		A138	GND
A069	ENET_TD3		A139	USB1_RX_N
A070	ENET_TD0		A140	USB1_RX_P

Table 34 Internal Pads

Pad #	MCM-iMX8M-Plus Signal Name		Pad #	MCM-iMX8M-Plus Signal Name
B001	GND		B059	GND
B002	EXT_NVCC_SNVS_1P8		B060	HDMI_HPD
B003	GPIO1_06		B061	HDMI_CEC
B004	GPIO1_05		B062	ECSPI2_SS0
B005	SAI5_RXD3		B063	ECSPI2_MOSI
B006	GPIO1_13		B064	ECSPI2_MISO
B007	GPIO1_15		B065	ECSPI2_SCLK
B008	GND		B066	GND
B009	GPIO1_00		B067	GPIO1_10
B010	GPIO1_08		B068	SAI2_RXD0
B011	GPIO1_07		B069	SAI3_MCLK

B012	GPIO1_01		B070	SAI3_RXFS
B013	GND		B071	GND
B014	I2C4_SDA		B072	SAI3_RXC
B015	I2C4_SCL		B073	SAI3_RXD
B016	GND		B074	SAI3_TXFS
B017	GPIO1_11		B075	GND
B018	V_SOM		B076	SAI3_TXC
B019	SAI5_RXD2		B077	SAI3_TXD
B020	USB1_TX_N		B078	GND
B021	USB1_TX_P		B079	SAI2_TXD0
B022	GND		B080	SAI2_MCLK
B023	NAND_ALE		B081	GND
B024	NAND_CE0_B		B082	SAI2_RXC
B025	NAND_DATA03		B083	SAI2_TXC
B026	NAND_DATA02		B084	GND
B027	NAND_DATA01		B085	UART1_RXD
B028	NAND_DATA00		B086	UART1_TXD
B029	GND		B087	GND
B030	GND		B088	GND
B031	LVDS0_D0_P		B089	ECSPI1_SCLK
B032	LVDS0_D0_N		B090	ECSPI1_SS0
B033	GND		B091	ECSPI1_MISO
B034	LVDS0_D1_P		B092	ECSPI1_MOSI
B035	LVDS0_D1_N		B093	GND
B036	GND		B094	SAI5_RXD0
B037	LVDS0_CLK_P		B095	SAI5_MCLK
B038	LVDS0_CLK_N		B096	SAI5_RXC
B039	GND		B097	SAI5_RXFS
B040	LVDS0_D2_P		B098	GND
B041	LVDS0_D2_N		B099	SAI1_RXD3
B042	GND		B100	SAI1_RXD2
B043	LVDS0_D3_P		B101	SAI1_RXD1
B044	LVDS0_D3_N		B102	SAI1_RXD0
B045	GND		B103	GND
B046	PMIC_ON_REQ		B104	SAI1_RXC
B047	SAI1_MCLK		B105	SAI1_RXFS
B048	QSPI_BOOT_EN_3P3		B106	GND
B049	EARC_N_HPD		B107	SAI1_TXD7
B050	GND		B108	SAI1_TXD6
B051	EARC_P_UTIL		B109	SAI2_RXFS
B052	HDMI_DDC_SCL		B110	SAI2_TXFS
B053	HDMI_DDC_SDA		B111	UART3_TXD
B054	GND		B112	UART3_RXD
B055	SPDIF_EXT_CLK		B113	GND
B056	SPDIF_RX		B114	I2C3_SDA
B057	SPDIF_TX		B115	I2C3_SCL
B058	GND		B116	GND

6.2 Heat Spreader and Cooling Solutions

MCM-iMX8M-Plus is provided with an optional heat-spreader assembly. The MCM-iMX8M-Plus heat-spreader is designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the MCM-iMX8M-Plus temperature specifications. Various thermal management solutions can be used, including active and passive heat dissipation approaches.

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 35 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	4.8	V
Voltage on any non-power supply pin	-0.5	3.6	V
Backup battery supply voltage (VCC_RTC)	-0.3	3.8	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 36 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.45	3.7	4.4	V
Backup battery supply voltage (VCC_RTC)	1.5	3.0	3.6	V

7.3 ESD Performance

Table 37 ESD Performance

Interface	ESD Performance
i.MX8M Plus pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)

8 MECHANICAL SPECIFICATIONS

8.1 Mechanical Drawings

3D model and mechanical drawings in DXF format are available at

https://www.compulab.com/products/computer-on-modules/mcm-imx8m-plus-nxp-i-mx-8m-plus-som-system-on-module-computer/#devres

8.2 Recommended Footprint

MCM-iMX8M-Plus footprint in DXF and HKP formats is available at

https://www.compulab.com/products/computer-on-modules/mcm-imx8m-plus-nxp-i-mx-8m-plus-som-system-on-module-computer/#devres

9 APPLICATION NOTES

9.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V_SOM and GND near the SOM.
- Except for a power connection, no other connection is mandatory for MCM-iMX8M-Plus operation. All power-up circuitry and all required pullups/pulldowns are available onboard MCM-iMX8M-Plus.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- Refer to the SBC-MCM8PLUS carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

9.2 Carrier Board Troubleshooting

- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches.
- Using an oscilloscope, verify that the GND pins are indeed at zero voltage level and that there is no ground bouncing.
- Create a "minimum system" - only power, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
  - Devices improperly driving the local bus
  - External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
  - Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between SOM pads. Even if the signals are not used on the carrier board, shorting them can disable the module operation. An initial

check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray. Note that solder shorts are the most probable factor to prevent a module from booting.

- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from MCM-iMX8M-Plus, or even damage the module hardware permanently.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.