UCM-iMX95

Reference Guide

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Table 1 Revision Notes

Date	Description
Oct 2024	• Initial release

Please check for a newer revision of this manual at the Compulab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program Compulab UCM-iMX95 System-on-Module.

1.2 UCM-iMX95 Part Number Legend

Please refer to the Compulab website 'Ordering information' section to decode the UCM-iMX95 part number: https://www.compulab.com/products/computer-on-modules/ucm-imx95-nxp-i-mx-95-som-system-on-module/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
UCM-iMX95 Developer Resources	https://www.compulab.com/products/computer-on-modules/ucm-imx95-nxp-i-mx-95-som-system-on-module/#devres
i.MX95 Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-9-processors/i-mx-95-applications-processor-family-high-performance-safety-enabled-platform-with-eiq-neutron-npu:iMX95
i.MX95 Datasheet	

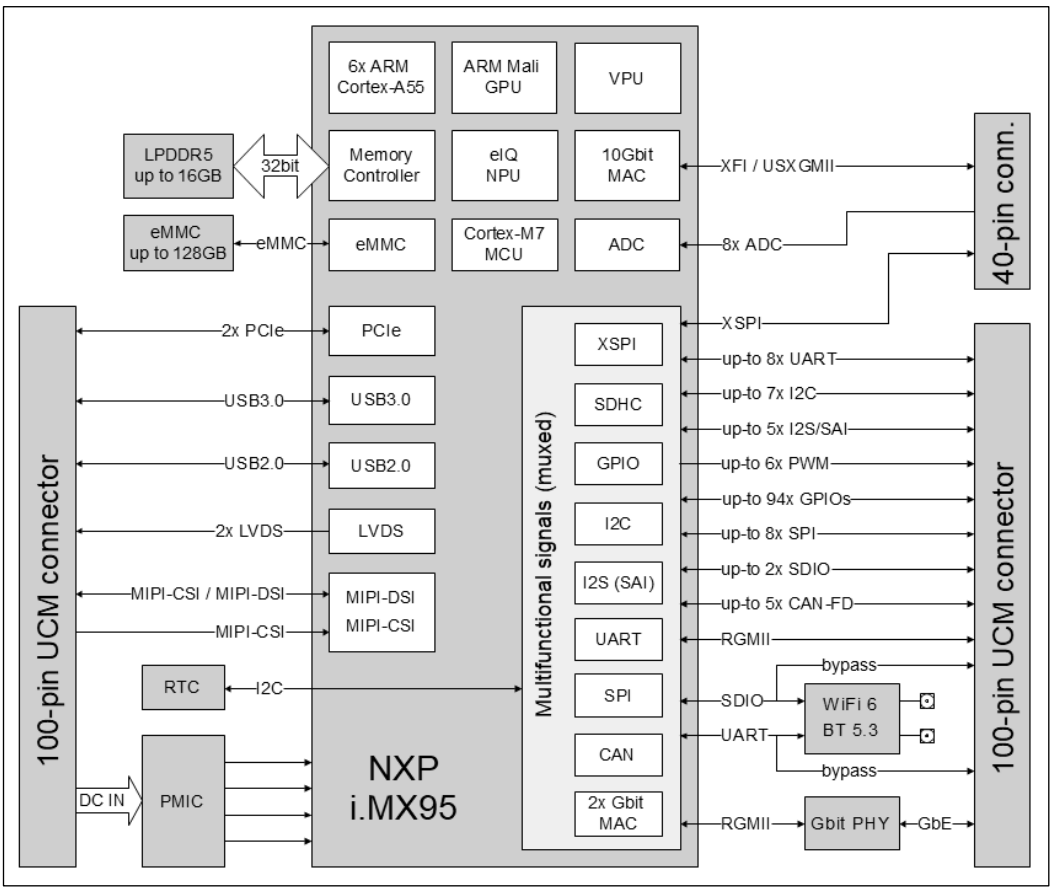
2 OVERVIEW

2.1 Highlights

- NXP i.MX95 processor, up-to 2.0 GHz
- Up to 16GB LPDDR5 and 128GB eMMC
- ARM Mali GPU and 4K VPU
- Integrated eIQ® Neutron NPU
- 2x LVDS, MIPI-DSI, 2x MIPI-CSI with ISP
- GbE + 10GbE, RGMII, 2x PCIe, USB3.0
- Certified 802.11ax WiFi, BT 5.3
- 5x CAN, 8x UART, 8x SPI, 75x GPIO
- Tiny size and weight - 28 x 40 x 5 mm, 12 gram

2.2 Block Diagram

Figure 1 UCM-iMX95 Block Diagram



2.3 Specifications

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX95, 6x ARM Cortex-A55, 1.8 GHz	C1800HM
VPU	4K video decode and encode	C1800HM
GPU	ARM Mali-G310 GPU OpenGL® ES 3.2, Vulkan® 1.2, OpenCL 3.0	+
NPU	eIQ® Neutron NPU	C1800HM
Real-Time Co-processor	ARM Cortex-M7 + ARM Cortex-M33	+
Memory and Storage		
RAM	2GB-16GB, LPDDR5	D
Storage	eMMC flash, 16GB - 128GB	N
Display, Camera and Audio		
Display	LVDS, 2x 4-lane or 1x 8-lane , up to 1080p60	+
	MIPI-DSI, 4 data lanes, up to 4kp30 or 3840x1440p60	+
Touchscreen	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	2x MIPI-CSI, 4 data lanes	+
Audio	Up-to 5x I2S / SAI	+
	S/PDIF input/output	+
Network		
Ethernet	Gigabit Ethernet port (MAC+PHY)	E
RGMII	Secondary RGMII	+
10 Gbit Ethernet	10 GbE MAC	+
WiFi	Certified 802.11ax WiFi	WB
Bluetooth	Bluetooth 5.3 BLE	
I/O		
PCI Express	2x PCIe Gen 3.0 1x lane	+
USB	1x USB3.0 + 1x USB2.0	+
UART	Up-to 8x UART	+
CAN bus	Up-to 5x CAN-FD	+
SD/SDIO	Up-to 2x SD/SDIO	+
SPI	Up to 8x SPI	+
I2C	Up to 7x I2C	+
ADC	8x general-purpose ADC channels	
PWM	Up to 6x PWM signals	+
GPIO	Up to 94x GPIO (multifunctional signals shared with other functions)	+
System Logic		
RTC	Real-time clock, powered by external battery	+

Feature	Description	Option
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

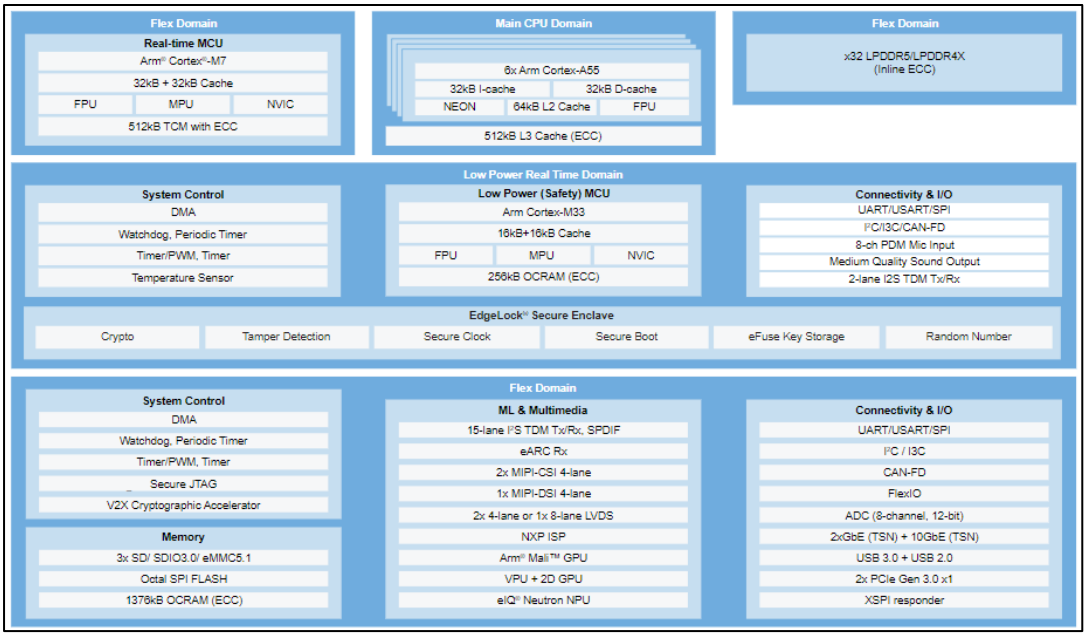
Electrical Specifications	
Supply Voltage	3.45V to 4.4V
Digital I/O voltage	3.3V / 1.8V
Mechanical Specifications	
Dimensions	28 x 40 x 5 mm
Weight	12 gram
Connectors	2 x 100 pin, 0.4mm pitch 1 x 40 pin, 0.4mm pitch - optional
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 i.MX95 System-on-Chip

The i.MX 95 System-on-Chip (SoC) includes powerful 6x Arm® Cortex®-A55 processors with speeds up to 2.0 GHz integrated with a NPU that accelerates machine learning inference. An Arm® Cortex®-M33 running up to 333 MHz and Cortex®-M7 running up to 800 MHz for real-time and low-power processing.

Figure 2 i.MX 95 Block Diagram



3.2 Memory

3.2.1 DRAM

UCM-iMX95 is equipped with up to 16GB of onboard LPDDR5 memory. The LPDDR5 channel is 32-bits wide.

3.2.2 Bootloader and General Purpose Storage

UCM-iMX95 uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is intended to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

UCM-iMX95 implements a variety of peripheral interfaces through two 100-pin (0.4mm pitch) and one 40-pin (0.4mm pitch) carrier board connectors. The following notes apply to interfaces available through the carrier-board connectors:

- Some interfaces/signals are available only with/without certain configuration options of the UCM-iMX95 SoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Some of the UCM-iMX95 carrier board interface pins are multifunctional. Up to 8 functions (ALT modes) are accessible through each multifunctional pin. For additional details, please refer to chapter 5.6.
- All of the UCM-iMX95 digital interfaces operate at 3.3V voltage levels unless noted otherwise.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** Pin number on the carrier board interface connector
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question
- **"Voltage Domain"** – Voltage level of the particular signal
- **"Availability" –** Depending on UCM-iMX95 configuration options, certain carrier board interface pins are physically disconnected (floating). The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"P"** – Power
- **"PD" -** Always pulled down onboard UCM-iMX95, followed by pull value.
- **"PU" -** Always pulled up onboard UCM-iMX95, followed by pull value.
- **"LVDS" -** Low-voltage differential signaling.

4.1 Display Interfaces

4.1.1 MIPI-DSI

The UCM-iMX95 MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX95 SoC. It is mutually exclusive with one CSI interface. Both DSI and CSI are routed directly to the carrier board interface. The following main features are supported:

- Compliant with MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2
- Maximum data rate per lane of 2.5 Gbps
- Resolution ranges: 4Kp30 or 3840 x 1440 p60

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes the MIPI-DSI interface signals.

Table 5 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
MIPI_DSICSI_CLK_N	P2-21	AO	Negative part of MIPI-DSICSI clock diff-pair	Always
MIPI_DSICSI_CLK_P	P2-23	AO	Positive part of MIPI-DSICSI clock diff-pair	Always
MIPI_DSICSI_D0_N	P2-1	AO	Negative part of MIPI-DSICSI data diff-pair 0	Always
MIPI_DSICSI_D0_P	P2-3	AO	Positive part of MIPI-DSICSI data diff-pair 0	Always
MIPI_DSICSI_D1_N	P2-15	AO	Negative part of MIPI-DSICSI data diff-pair 1	Always
MIPI_DSICSI_D1_P	P2-17	AO	Positive part of MIPI-DSICSI data diff-pair 1	Always
MIPI_DSICSI_D2_N	P2-5	AO	Negative part of MIPI-DSICSI data diff-pair 2	Always
MIPI_DSICSI_D2_P	P2-7	AO	Positive part of MIPI-DSICSI data diff-pair 2	Always
MIPI_DSICSI_D3_N	P2-11	AO	Negative part of MIPI-DSICSI data diff-pair 3	Always
MIPI_DSICSI_D3_P	P2-13	AO	Positive part of MIPI-DSICSI data diff-pair 3	Always

4.1.2 LVDS Interface

UCM-iMX95 provides a dual LVDS interface derived from the i.MX95 LVDS display bridge. It supports the following key features:

- 2x 4-lane or 1x 8-lane operation modes
- Resolutions of up to 1080p60

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes the LVDS interface signals.

Table 6 LVDS Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS0_CLK_N	P1-82	AO	Negative part of LVDS0 clock diff-pair	Always
LVDS0_CLK_P	P1-80	AO	Positive part of LVDS0 clock diff-pair	Always
LVDS0_D0_N	P1-44	AO	Negative part of LVDS0 data diff-pair 0	Always
LVDS0_D0_P	P1-42	AO	Positive part of LVDS0 data diff-pair 0	Always
LVDS0_D1_N	P1-48	AO	Negative part of LVDS0 data diff-pair 1	Always
LVDS0_D1_P	P1-46	AO	Positive part of LVDS0 data diff-pair 1	Always
LVDS0_D2_N	P1-52	AO	Negative part of LVDS0 data diff-pair 2	Always
LVDS0_D2_P	P1-50	AO	Positive part of LVDS0 data diff-pair 2	Always
LVDS0_D3_N	P1-58	AO	Negative part of LVDS0 data diff-pair 3	Always
LVDS0_D3_P	P1-56	AO	Positive part of LVDS0 data diff-pair 3	Always
LVDS1_CLK_N	P2-58	AO	Negative part of LVDS1 clock diff-pair	Always
LVDS1_CLK_P	P2-56	AO	Positive part of LVDS1 clock diff-pair	Always

Signal Name	Pin #	Type	Description	Availability
LVDS1_D0_N	P2-14	AO	Negative part of LVDS1 data diff-pair 0	Always
LVDS1_D0_P	P2-12	AO	Positive part of LVDS1 data diff-pair 0	Always
LVDS1_D1_N	P2-20	AO	Negative part of LVDS1 data diff-pair 1	Always
LVDS1_D1_P	P2-18	AO	Positive part of LVDS1 data diff-pair 1	Always
LVDS1_D2_N	P2-26	AO	Negative part of LVDS1 data diff-pair 2	Always
LVDS1_D2_P	P2-24	AO	Positive part of LVDS1 data diff-pair 2	Always
LVDS1_D3_N	P2-50	AO	Negative part of LVDS1 data diff-pair 3	Always
LVDS1_D3_P	P2-48	AO	Positive part of LVDS1 data diff-pair 3	Always

4.2 Camera Interface

UCM-iMX95 provides two MIPI-CSI interfaces, derived from the MIPI CSI host controllers integrated into the i.MX95 SoC. One MIPI-CSI interface is mutually exclusive with MIPI-DSI interface. Both DSI and CSI are routed directly to the carrier board interface. The following main features are supported:

- Up-to four data lanes and one clock lane for each interface
- Complaint with MIPI CSI-2 specification v2.0 and MIPI D-PHY specification v1.2

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes MIPI-CSI signals.

Table 7 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
MIPI_DSICSI_CLK_N	P2-21	AO	Negative part of MIPI-DSICSI clock diff-pair	Always
MIPI_DSICSI_CLK_P	P2-23	AO	Positive part of MIPI- DSICSI clock diff-pair	Always
MIPI_DSICSI_D0_N	P2-1	AO	Negative part of MIPI- DSICSI data diff-pair 0	Always
MIPI_DSICSI_D0_P	P2-3	AO	Positive part of MIPI- DSICSI data diff-pair 0	Always
MIPI_DSICSI_D1_N	P2-15	AO	Negative part of MIPI- DSICSI data diff-pair 1	Always
MIPI_DSICSI_D1_P	P2-17	AO	Positive part of MIPI- DSICSI data diff-pair 1	Always
MIPI_DSICSI_D2_N	P2-5	AO	Negative part of MIPI- DSICSI data diff-pair 2	Always
MIPI_DSICSI_D2_P	P2-7	AO	Positive part of MIPI- DSICSI data diff-pair 2	Always
MIPI_DSICSI_D3_N	P2-11	AO	Negative part of MIPI- DSICSI data diff-pair 3	Always
MIPI_DSICSI_D3_P	P2-13	AO	Positive part of MIPI- DSICSI data diff-pair 3	Always
MIPI_CSI_CLK_N	P2-2	AO	Negative part of MIPI-CSI clock diff-pair	Always
MIPI_CSI_CLK_P	P2-4	AO	Positive part of MIPI- CSI clock diff-pair	Always
MIPI_CSI_D0_N	P2-6	AO	Negative part of MIPI- CSI data diff-pair 0	Always
MIPI_CSI_D0_P	P2-8	AO	Positive part of MIPI- CSI data diff-pair 0	Always
MIPI_CSI_D1_N	P2-31	AO	Negative part of MIPI- CSI data diff-pair 1	Always
MIPI_CSI_D1_P	P2-33	AO	Positive part of MIPI- CSI data diff-pair 1	Always
MIPI_CSI_D2_N	P2-25	AO	Negative part of MIPI- CSI data diff-pair 2	Always
MIPI_CSI_D2_P	P2-27	AO	Positive part of MIPI- CSI data diff-pair 2	Always
MIPI_CSI_D3_N	P2-35	AO	Negative part of MIPI- CSI data diff-pair 3	Always
MIPI_CSI_D3_P	P2-37	AO	Positive part of MIPI- CSI data diff-pair 3	Always

4.3 Audio Interfaces

4.3.1 S/PDIF

UCM-iMX95 provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes the S/PDIF interface signals.

Table 8 S/PDIF Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SPDIF_IN	P1-79	I	SPDIF input data line signal	3.3V	Always
	P2-43			ENET	
	P2-47			ENET	
SPDIF_OUT	P1-81	O	SPDIF output data line signal	3.3V	Always
	P2-47			ENET	

NOTE: When the SOM is assembled with the "E" configuration option (on-board PHY), signals that belong to "ENET" domain operate at 3.3V voltage levels. When the SOM is assembled without the "E" configuration option, voltage level of "ENET" signals is controlled by EXT_ENET pin (P1-55).

NOTE: S/PDIF signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.3.2 SAI

UCM-iMX95 supports up-to five of the i.MX95 integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 2 data lines. One receiver with independent bit clock and frame sync supporting 2 data lines.
- Maximum Frame Size of 32 words per data line.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive data line

Please refer to the i.MX95 Reference manual for additional details. The tables below summarize the SAI interface signals.

Table 9 SAI1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SAI1_MCLK	P1-84	IO	Audio master clock. An input when generated externally and an output when generated internally.	3.3V	Always
	P1-98			3.3V	Always
SAI1_RX_DATA[0]	P1-98	I	Receive data, sampled synchronously by the bit clock	3.3V	Always
SAI1_TX_DATA[0]	P1-92	O	Transmit data signal synchronous to bit clock.	3.3V	Always

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SAI1_TX_DATA[1]	P1-95	O	Transmit data signal synchronous to bit clock.	3.3V	Always
SAI1_TXC	P1-70	O	Transmit bit clock. An input when generated externally and an output when generated internally.	3.3V	Always
SAI1_TXFS	P1-95	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	3.3V	Always

NOTE: SAI1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 10 SAI2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SAI2_MCLK	P2-45	IO	Audio master clock. An input when generated externally and an output when generated internally.	ENET	Always
SAI2_RX_DATA[0]	P2-65	I	Receive data, sampled synchronously by the bit clock	ENET	Always
SAI2_RX_DATA[1]	P2-63	I	Receive data, sampled synchronously by the bit clock	ENET	Always
SAI2_RX_DATA[2]	P2-61	I	Receive data, sampled synchronously by the bit clock	ENET	Always
SAI2_RX_DATA[3]	P2-59	I	Receive data, sampled synchronously by the bit clock	ENET	Always
SAI2_RX_BCLK	P2-60	I	Receive bit clock. An input when generated externally and an output when generated internally.	ENET	Always
SAI2_RXFS	P2-76	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	ENET	Always
SAI2_TX_DATA[0]	P2-53	O	Transmit data signal synchronous to bit clock.	ENET	Always
SAI2_TX_DATA[1]	P2-55	O	Transmit data signal synchronous to bit clock.	ENET	Always
SAI2_TX_DATA[2]	P2-41	O	Transmit data signal synchronous to bit clock.	ENET	Always
SAI2_TX_DATA[3]	P2-43	O	Transmit data signal synchronous to bit clock.	ENET	Always
SAI2_TX_DATA[4]	P3-10 P3-22	O	Transmit data signal synchronous to bit clock.	1.8V	Always
SAI2_TX_DATA[5]	P3-20 P3-24	O	Transmit data signal synchronous to bit clock.	1.8V	Always
SAI2_TX_DATA[6]	P3-14 P3-28 P3-36	O	Transmit data signal synchronous to bit clock.	1.8V	Always
SAI2_TX_DATA[7]	P3-16 P3-30 P3-38	O	Transmit data signal synchronous to bit clock.	1.8V	Always
SAI2_TX_BCLK	P2-69	O	Transmit bit clock. An input when generated externally and an output when generated internally.	ENET	Always

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SAI2_TXFS	P2-67	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	ENET	Always

NOTE: When the SOM is assembled with the "E" configuration option (on-board PHY), signals that belong to "ENET" domain operate at 3.3V voltage levels. When the SOM is assembled without the "E" configuration option, voltage level of "ENET" signals is controlled by EXT_ENET pin (P1-55).

NOTE: SAI2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 11 SAI3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SAI3_MCLK	P1-30	IO	Audio master clock. An input when generated externally and an output when generated internally.	3.3V	Always
				3.3V	Always
SAI3_RX_BCLK	P1-26	I	Receive bit clock. An input when generated externally and an output when generated internally.	3.3V	Always
	P1-32				
SAI3_RXFS	P1-34	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	3.3V	Always
	P1-35				
SAI3_RX_DATA[0]	P1-28	I	Receive data, sampled synchronously by the bit clock	3.3V	Always
SAI3_TX_DATA[0]	P1-26	O	Transmit data signal synchronous to bit clock.	3.3V	Always
	P1-34				
SAI3_TX_BCLK	P1-36	O	Transmit bit clock. An input when generated externally and an output when generated internally.	3.3V	Always
SAI3_TXFS	P1-38	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	3.3V	Always

NOTE: SAI3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 12 SAI4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SAI4_RX_BCLK	P2-41	I	Receive bit clock. An input when generated externally and an output when generated internally.	ENET	Always
	P3-20			1.8V	
SAI4_RXFS	P2-55	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	ENET	Always
	P3-10			1.8V	
SAI4_RX_DATA[0]	P2-43	I	Receive data, sampled synchronously by the bit clock	ENET	Always
	P3-30			1.8V	
SAI4_RX_DATA[1]	P3-22	I	Receive data, sampled synchronously by the bit clock	1.8V	Always

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SAI4_TX_DATA[0]	P2-59	O	Transmit data signal synchronous to bit clock.	ENET	Always
	P3-28			1.8V	
SAI4_TX_DATA[1]	P3-24	O	Transmit data signal synchronous to bit clock.	1.8V	Always
SAI4_TX_BCLK	P2-61	O	Transmit bit clock. An input when generated externally and an output when generated internally.	ENET	Always
	P3-22			1.8V	
SAI4_TXFS	P2-63	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	ENET	Always
	P3-24			1.8V	

NOTE: When the SOM is assembled with the "E" configuration option (on-board PHY), signals that belong to "ENET" domain operate at 3.3V voltage levels. When the SOM is assembled without the "E" configuration option, voltage level of "ENET" signals is controlled by EXT_ENET pin (P1-55).

NOTE: SAI4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 13 SAI5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SAI5_RX_DATA[0]	P1-75	I	Receive data, sampled synchronously by the bit clock	1.8V	Only w/o 'WB' option
	P3-40				Always
SAI5_RX_DATA[1]	P1-60	I	Receive data, sampled synchronously by the bit clock	1.8V	Only w/o 'WB' option
	P3-32				Always
SAI5_RX_DATA[2]	P1-62	I	Receive data, sampled synchronously by the bit clock	1.8V	Only w/o 'WB' option
	P3-36				Always
SAI5_RX_DATA[3]	P1-63	I	Receive data, sampled synchronously by the bit clock	1.8V	Only w/o 'WB' option
	P3-38				Always
SAI5_RX_BCLK	P1-59	I	Receive bit clock. An input when generated externally and an output when generated internally.	1.8V	Only w/o 'WB' option
	P3-16				Always
SAI5_RXFS	P1-77	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	1.8V	Only w/o 'WB' option
	P3-14				Always
SAI5_TX_DATA[0]	P1-60	O	Transmit data signal synchronous to bit clock.	1.8V	Only w/o 'WB' option
	P3-32				Always
SAI5_TX_DATA[1]	P1-75	O	Transmit data signal synchronous to bit clock.	1.8V	Only w/o 'WB' option
	P3-40				Always
SAI5_TX_DATA[2]	P1-77	O	Transmit data signal synchronous to bit clock.	1.8V	Only w/o 'WB' option
	P3-14				Always

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SAI5_TX_DATA[3]	P1-59	O	Transmit data signal synchronous to bit clock.	1.8V	Only w/o 'WB' option
	P3-16				Always
SAI5_TX_BCLK	P1-63	O	Transmit bit clock. An input when generated externally and an output when generated internally.	1.8V	Only w/o 'WB' option
	P3-38				Always
SAI5_TXFS	P1-62	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	1.8V	Only w/o 'WB' option
	P3-36				Always

NOTE: SAI5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.3.3 MQS

UCM-iMX95 supports up-to two MOQ interfaces that can be used to generate medium quality audio via standard GPIO.

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes the S/PDIF interface signals.

Table 14 MQS Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
MQS1_LEFT	P1-95	O	Left signal output	3.3V	Always
	P3-2			3.3V	Always
MQS1_RIGHT	P1-98	O	Right signal output	3.3V	Always
	P3-4			3.3V	Always
MQS2_LEFT	P1-71	O	Left signal output	1.8	Always
	P2-47			1.8	Always
	P2-98			SD2	
MQS2_RIGHT	P1-67	O	Right signal output	1.8	Always
	P2-45			1.8	Always
	P2-94			SD2	

NOTE: Pins that belong to the "SD2" domain can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL (GPIO3_IO19).

NOTE: MQS signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.3.4 PDM

UCM-iMX95 supports up-to four microphone PDM interfaces that delivers audio from microphones to the processor.

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes the PDM interface signals.

Table 15 PDM Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
PDM_CLK	P1-26 P2-91 P3-2	I	Clock signal that synchronizes the generation and processing of the PDM bit streams	3.3V	Always
PDM_BIT_STREAM0	P1-28 P2-89 P3-4	I	PDM input channel 0	3.3V	Always
PDM_BIT_STREAM1	P1-38 P2-95 P3-6	I	PDM input channel 1	3.3V	Always
PDM_BIT_STREAM2	P1-35 P1-36	I	PDM input channel 2	3.3V	Always
PDM_ BIT_STREAM3	P1-34 P1-37	I	PDM input channel 3	3.3V	Always

NOTE: PDM signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.4 Ethernet

4.4.1 10 Gigabit Ethernet

UCM-iMX95 provides one 10 Gigabit Ethernet controller. The controller supports XFI, SGMII (2.5G and 1G), and 10G-USXGMII (single 10GE mode only).

The tables below summarize the 10GbE interface signals.

Table 16 10GbE Interface Signals

Signal Name	Pin #	Type	Description	Availability
ETH_CLKIN_N	P3-27	I	10GbE reference clock negative	Always
ETH_CLKIN_P	P3-25	I	10GbE reference clock positive	Always
ETH_RX0_N	P3-39	I	10GbE receive data negative	Always
ETH_RX0_P	P3-37	I	10GbE receive data positive	Always
ETH_TX0_N	P3-33	O	10GbE transmit data negative	Always
ETH_TX0_P	P3-31	O	10GbE transmit data positive	Always

4.4.2 Gigabit Ethernet

UCM-iMX95 incorporates an optional ("E" configuration option) full-featured 10/100/1000 Ethernet interface implemented with Realtek RTL8211FD GbE PHY.

The following main features are supported:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- IEEE 802.3u compliant Auto-Negotiation
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- Activity and speed indicator LED controls

The table below summarizes the GbE interface signals.

Table 17 GbE Interface Signals

Signal Name	Pin #	Type	Description	Availability
ETH1_LED1/CFG_LDO0	P2-83	O	Active High, activity LED driver. 3.3V signal	With 'E' option
ETH1_LED0/CFG_EXT	P2-86	O	Active low, link, any speed LED driver. 3.3V signal	With 'E' option
ETH1_LED2/CFG_LDO1	P2-75	O	Active High, link, any speed , blinking on transmit or receive	With 'E' option
ETH1_MDI0N	P2-73	IO	Negative part of 100ohm diff-pair 0	With 'E' option
ETH1_MDI0P	P2-74	IO	Positive part of 100ohm diff-pair 0	With 'E' option
ETH1_MDI1N	P2-80	IO	Negative part of 100ohm diff-pair 1	With 'E' option
ETH1_MDI1P	P2-78	IO	Positive part of 100ohm diff-pair 1	With 'E' option
ETH1_MDI2N	P2-81	IO	Negative part of 100ohm diff-pair 2	With 'E' option
ETH1_MDI2P	P2-79	IO	Positive part of 100ohm diff-pair 2	With 'E' option
ETH1_MDI3N	P2-85	IO	Negative part of 100ohm diff-pair 3	With 'E' option
ETH1_MDI3P	P2-84	IO	Positive part of 100ohm diff-pair 3	With 'E' option

4.4.3 RGMII

UCM-iMX95 features one RMGII interface.

The tables below summarize the Ethernet RGMII interface signals.

Table 18 RGMII ENET2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
ENET2_MDC	P2-76	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	ENET	Always
ENET2_MDIO	P2-60	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	ENET	Always
ENET2_RD0	P2-41	I	Ethernet input data from the PHY	ENET	Always
ENET2_RD1	P2-43	I	Ethernet input data from the PHY	ENET	Always
ENET2_RD2	P2-45	I	Ethernet input data from the PHY	ENET	Always
ENET2_RD3	P2-47	I	Ethernet input data from the PHY	ENET	Always
ENET2_RX_CTL	P2-53	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	ENET	Always
ENET2_RXC	P2-55	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	ENET	Always

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
ENET2_TD0	P2-59	O	Ethernet output data to PHY	ENET	Always
ENET2_TD1	P2-61	O	Ethernet output data to PHY	ENET	Always
ENET2_TD2	P2-63	O	Ethernet output data to PHY	ENET	Always
ENET2_TD3	P2-65	O	Ethernet output data to PHY	ENET	Always
ENET2_TXC	P2-69	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	ENET	Always
ENET2_TX_CTL	P2-67	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	ENET	Always

NOTE: When the SOM is assembled with the "E" configuration option (on-board PHY), signals that belong to "ENET" domain operate at 3.3V voltage levels. When the SOM is assembled without the "E" configuration option, voltage level of "ENET" signals is controlled by EXT_ENET pin (P1-55).

NOTE: ENET2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.5 PCI-Express

UCM-iMX95 provides two PCI Express Gen 3.0 ports.

The following tables summarize the PCIe interface signals.

Table 19 PCIE1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE_CLKOUT_N	P1-25	O	100 MHz PCIe reference clock differential output negative	Always available
PCIE_CLKOUT_P	P1-23	O	100 MHz PCIe reference clock differential output positive	Always available
PCIE1_CLKIN_N	P2-44	I	100 MHz PCIe reference clock differential input negative	Always available
PCIE1_CLKIN_P	P2-42	I	100 MHz PCIe reference clock differential input positive	Always available
PCIE1_RX0_N	P2-30	I	PCI Express receive data negative	Always available
PCIE1_RX0_P	P2-32	I	PCI Express receive data positive	Always available
PCIE1_TX0_N	P2-36	O	PCI Express transmit data negative	Always available
PCIE1_TX0_P	P2-38	O	PCI Express transmit data positive	Always available
PCIE1_CLK_REQ	P2-90	O	PCI Express Enable external clock generator	Always available

NOTE: PCIE1_CLK_REQ signal is multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 20 PCIE2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE_CLKOUT_N	P1-25	O	100 MHz PCIe reference clock differential output negative	Always available
PCIE_CLKOUT_P	P1-23	O	100 MHz PCIe reference clock differential output positive	Always available
PCIE2_CLKIN_N	P1-31	I	100 MHz PCIe reference clock differential input negative	Always available

Signal Name	Pin #	Type	Description	Availability
PCIE2_CLKIN_P	P1-29	I	100 MHz PCIe reference clock differential input positive	Always available
PCIE2_RX0_N	P1-47	I	PCI Express receive data negative	Always available
PCIE2_RX0_P	P1-45	I	PCI Express receive data positive	Always available
PCIE2_TX0_N	P1-41	O	PCI Express transmit data negative	Always available
PCIE2_TX0_P	P1-39	O	PCI Express transmit data positive	Always available
PCIE2_CLK_REQ	P1-85	O	PCI Express Enable external clock generator	Always available

NOTE: PCIE2_CLK_REQ signal is multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.6 WiFi and Bluetooth

UCM-iMX95 features optional 802.11ax WiFi and Bluetooth functions implemented with the Ezurio SONA NX611 certified WiFi module (NXP IW611 chipset).

The module provides the following key features:

- IEEE 802.11 ax/ac/a/b/g/n, Wi-Fi compliant
- Bluetooth 5.4 complaint

The wireless module is interfaced with i.MX95 SoC through SDIO3 interface.

The wireless module provides two on-board MHF4 antenna connectors:

- J1 – 2.4GHz WiFi / Bluetooth antenna
- J2 – auxiliary 2.4GHz / 5GHz WiFi antenna

NOTE: WiFi and Bluetooth functions are available only with "WB" configuration option.

4.7 USB

UCM-iMX95 provides one USB3.0 port and one USB2.0 port. Both can be configured as host or device. USB3.0 integrates two pairs of TX/RX signals which can be connected to a type-C connector directly without external high-speed switch chip.

Please refer to the i.MX95 Reference manual for additional details.

The tables below summarize the USB interface signals.

Table 21 USB port #1 Signals

Signal Name	Pin #	Type	Description	Availability
USB1_DN	P1-14	IO	USB2.0 negative data	Always available
USB1_DP	P1-12	IO	USB2.0 positive data	Always available
USB1_VBUS	P1-24	I	USB1 VBUS detect	Always available
USB1_ID	P1-22	I	USB1 ID	Always available
USB1_TX0_N	P1-18	AO	USB3.0 transmit negative lane	Always available
USB1_TX0_P	P1-16	AO	USB3.0 transmit positive lane	Always available
USB1_RX0_N	P1-8	AI	USB3.0 receive negative lane	Always available
USB1_RX0_P	P1-6	AI	USB3.0 receive positive lane	Always available
USB1_TX1_N	P1-15	AO	USB3.0 transmit negative lane	Always available

Signal Name	Pin #	Type	Description	Availability
USB1_TX1_P	P1-13	AO	USB3.0 transmit positive lane	Always available
USB1_RX1_N	P1-9	AI	USB3.0 receive negative lane	Always available
USB1_RX1_P	P1-7	AI	USB3.0 receive positive lane	Always available

Table 22 USB port #2 Signals

Signal Name	Pin #	Type	Description	Availability
USB2_DN	P1-5	IO	USB2.0 negative data	Always available
USB2_DP	P1-3	IO	USB2.0 positive data	Always available
USB2_VBUS	P1-1	I	USB2 VBUS detect	Always available
USB2_ID	P1-17	I	USB2 ID	Always available

4.8 MMC / SD /SDIO

UCM-iMX95 features two SD/SDIO ports. These ports are derived from the i.MX95 uSDHC2 and uSDHC3 controllers. uSDHC IP supports the following main features:

- Fully compliant with MMC 5.1 command/response sets and physical layer
- Fully compliant with SD 3.0 command/response sets and physical layer

Please refer to the i.MX95 Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals.

Table 23 SD2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SD2_CLK	P2-96	O	Clock for MMC/SD/SDIO card	SD2	Always available
SD2_CMD	P2-100	IO	CMD line connect to card	SD2	Always available
SD2_DATA0	P2-97	IO	DATA0 line in all modes. Also used to detect busy state	SD2	Always available
SD2_DATA1	P2-99	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	SD2	Always available
SD2_DATA2	P2-94	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	SD2	Always available
SD2_DATA3	P2-98	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	SD2	Always available
SD2_RESET#	P2-51	O	Card hardware reset signal, active LOW	SD2	Always available
SD2_CD#	P2-92	I	Card detection pin	SD2	Always available

NOTE: SD2 pins can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL (GPIO3_IO19).

NOTE: SD2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 24 SD3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SD3_CLK	P1-75	O	Clock for MMC/SD/SDIO card	1.8V	Only w/o 'WB' option
	P1-79			3.3V	Always

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SD3_CMD	P1-77	IO	CMD line connect to card	1.8V	Only w/o 'WB' option
	P1-81			3.3V	Always
SD3_DATA0	P1-59	IO	DATA0 line in all modes. Also used to detect busy state	1.8V	Only w/o 'WB' option
SD3_DATA1	P1-33	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	3.3V	Always
	P1-60			1.8V	Only w/o 'WB' option
SD3_DATA2	P1-38	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	3.3V	Always
	P1-62			1.8V	Only w/o 'WB' option
SD3_DATA3	P1-49	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	3.3V	Always
	P1-63			1.8V	Only w/o 'WB' option

NOTE: SD3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.9 FlexSPI

UCM-iMX95 provides one FlexSPI port that can support 8-bit serial flash memory or serial RAM devices. Please refer to the i.MX95 Reference manual for additional details.

The table below summarizes the FlexSPI interface signals.

Table 25 FlexSPI Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
XSPI_CLK	P3-10	O	Flash serial clock	1.8V	Always
	P1-75				Only w/o 'WB' option
XSPI_SS0_B	P3-20	O	Flash chip select0	1.8V	Always
	P1-77				Only w/o 'WB' option
XSPI_SS1_B	P3-16	O	Flash chip select1	1.8V	Always
XSPI_DQS	P3-14	I	Flash data strobe	1.8V	Always
XSPI_DATA0	P3-22	IO	Flash data 0	1.8V	Always
	P1-59				Only w/o 'WB' option
XSPI_DATA1	P3-24	IO	Flash data 1	1.8V	Always
	P1-60				Only w/o 'WB' option
XSPI_DATA2	P3-28	IO	Flash data 2	1.8V	Always
	P1-62				Only w/o 'WB' option
XSPI_DATA3	P3-30	IO	Flash data 3	1.8V	Always
	P1-63				Only w/o 'WB' option
XSPI_DATA4	P3-32	IO	Flash data 4	1.8V	Always
XSPI_DATA5	P3-36	IO	Flash data 5	1.8V	Always
XSPI_DATA6	P3-38	IO	Flash data 6	1.8V	Always
XSPI_DATA7	P3-40	IO	Flash data 7	1.8V	Always

NOTE: FlexSPI signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.10 UART

UCM-iMX95 features up-to 8 UART ports. The i.MX95 UART supports the following features:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 5 Mbps.
- Hardware flow control support for a request to send and clear to send signals.

NOTE: By default UART1 is assigned to be used as the main system console port.

NOTE: By default UART2 is assigned to be used as the M33 core debug port.

Please refer to the i.MX95 Reference manual for additional details.

The tables below summarize the UART interface signals.

Table 26 UART1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
UART1_CTS	P1-84	O	Clear to send	3.3V	Always
UART1_RTS	P1-86	I	Request to send	3.3V	Always
UART1_DSR	P1-70	I	Data set ready	3.3V	Always
UART1_DTR	P1-92	O	Data terminal ready	3.3V	Always
UART1_RXD	P1-76	I	Serial data receive	3.3V	Always
UART1_TXD/BT_MODE0	P1-74	O	Serial data transmit	3.3V	Always

NOTE: UART1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 27 UART2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
UART2_CTS	P1-70	O	Clear to send	3.3V	Always
UART2_RTS	P1-92	I	Request to send	3.3V	Always
UART2_DSR	P1-98	I	Data set ready	3.3V	Always
UART2_DTR	P1-95	O	Data terminal ready	3.3V	Always
UART2_RXD	P1-84	I	Serial data receive	3.3V	Always
UART2_TXD/BT_MODE1	P1-86	O	Serial data transmit	3.3V	Always

NOTE: UART2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 28 UART3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
UART3_CTS	P1-36	O	Clear to send	3.3V	Always
UART3_RTS	P1-30	I	Request to send	3.3V	Always
UART3_RX	P1-19	I	Serial data receive	3.3V	Always
UART3_TX	P1-72	O	Serial data transmit	3.3V	Always

NOTE: UART3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 29 UART4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
UART4_RXD	P1-19	I	Serial data receive	3.3V	Always
	P2-41			ENET	Always
UART4_TXD	P1-72	O	Serial data transmit	3.3V	Always
	P2-59			ENET	Always
UART4_CTS	P1-36	O	Clear to send	3.3V	Always
	P2-45			ENET	Always
UART4_RTS	P1-30	I	Request to send	3.3V	Always
	P2-61			ENET	Always
UART4_DTR	P2-67	O	Data terminal ready	ENET	Always
UART4_DSR	P2-53	I	Data set ready	ENET	Always
UART4_RIN	P2-60	I	Receive interrupt number	ENET	Always
UART4_DCB	P2-76	O	Device control block	ENET	Always

NOTE: When the SOM is assembled with the "E" configuration option (on-board PHY), signals that belong to "ENET" domain operate at 3.3V voltage levels. When the SOM is assembled without the "E" configuration option, voltage level of "ENET" signals is controlled by EXT_ENET pin (P1-55).

NOTE: UART4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 30 UART5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
UART5_RX	P1-21	I	UART-5 serial data receive	3.3V	Only w/o 'WB' option
	P1-71			1.8V	Always
UART5_TX	P1-61	O	UART-5 serial data transmit	3.3V	Only w/o 'WB' option
	P1-67			1.8V	Always
UART5_CTS_B	P1-89	O	UART-5 clear to send	3.3V	Only w/o 'WB' option
	P1-73			1.8V	Always
UART5_RTS_B	P1-87	I	UART-5 request to send	3.3V	Only w/o 'WB' option
	P1-65			1.8V	Always

NOTE: UART5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 31 UART6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
UART6_RXD	P2-89	I	Serial data receive	3.3V	Always
UART6_TXD	P2-91 P2-90	O	Serial data transmit	3.3V	Always
UART6_CTS	P2-95	O	Clear to send	3.3V	Always
UART6_RTS	P2-93 P1-85	I	Request to send	3.3V	Always

NOTE: UART6 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 32 UART7 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
UART7_RXD	P1-99	I	Serial data receive	3.3V	Always
UART7_TXD	P1-97	O	Serial data transmit	3.3V	Always
UART7_CTS	P1-96	O	Clear to send	3.3V	Always
UART7_RTS	P1-100	I	Request to send	3.3V	Always

NOTE: UART7 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 33 UART8 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
UART8_RXD	P1-37	I	Serial data receive	3.3V	Always
UART8_TXD	P1-35	O	Serial data transmit	3.3V	Always
UART8_CTS	P1-72	O	Clear to send	3.3V	Always
UART8_RTS	P1-19	I	Request to send	3.3V	Always

NOTE: UART8 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.11 CAN-FD

UCM-iMX95 features up-to five CAN-FD interfaces. These interfaces support the following key features:

- Full implementation of the CAN FD protocol and CAN protocol specification version 2.0B
- Compliant with the ISO 11898-1 standard

Please refer to the i.MX95 Reference manual for additional details.

The tables below summarize the CAN interface signals.

Table 34 CAN1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
CAN1_TX	P1-92	O	CAN transmit pin	3.3V	Always
	P3-2			3.3V	
CAN1_RX	P1-70	I	CAN receive pin	3.3V	Always
	P3-4			3.3V	

NOTE: CAN1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 35 CAN2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
CAN2_TX	P1-33	O	CAN transmit pin	3.3V	Always
	P1-71			1.8V	Always
	P2-97			SD2	Always
CAN2_RX	P1-49	I	CAN receive pin	3.3V	Always
	P1-67			1.8V	Always
	P2-99			SD2	Always

NOTE: CAN2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pins denoted “SD2” can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL (GPIO3_IO19).

Table 36 CAN3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
CAN3_TX	P1-91	O	CAN transmit pin	3.3V	Always
	P2-49			1.8V	Always
CAN3_RX	P1-94	I	CAN receive pin	3.3V	Always
	P2-52			1.8V	Always

NOTE: CAN3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 37 CAN4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
CAN4_TX	P2-91	O	CAN transmit pin	3.3V	Always
	P1-65			1.8V	Always
CAN4_RX	P2-89	I	CAN receive pin	3.3V	Always
	P1-73			1.8V	Always

NOTE: CAN4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 38 CAN5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
CAN5_TX	P1-79	O	CAN transmit pin	3.3V	Always
	P1-51			3.3V	Always
CAN5_RX	P1-81	I	CAN receive pin	3.3V	Always
	P1-53			3.3V	Always

NOTE: CAN5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.12 SPI

Up-to eight SPI interfaces are accessible through the UCM-iMX95 carrier board interface. The SPI interfaces are derived from i.MX95 integrated low-power SPI modules. The following key features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Direct Memory Access (DMA) support

Please refer to the i.MX95 Reference manual for additional details.

The following tables summarize the SPI interface signals.

Table 39 SPI1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SPI1_SIN	P1-70	I	Serial data input	3.3V	Always
SPI1_SOUT	P1-98	O	Master data out; slave data in	3.3V	Always
SPI1_SCLK	P1-92	O	Master clock out; slave clock in	3.3V	Always
SPI1_PCS0	P1-95	O	Chip select 0	3.3V	Always
SPI1_PCS1	P3-4	O	Chip select 1	3.3V	Always

NOTE: SPI1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 40 SPI2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SPI2_SIN	P1-76	I	Master data in; slave data out	3.3V	Always
SPI2_SOUT	P1-84	O	Master data out; slave data in	3.3V	Always
SPI2_SCLK	P1-86	O	Master clock out; slave clock in	3.3V	Always
SPI2_PCS0	P1-74	O	Chip select 0	3.3V	Always
SPI2_PCS1	P3-6	O	Chip select 1	3.3V	Always

NOTE: SPI2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 41 SPI3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SPI3_SIN	P1-99	I	Master data in; slave data out	3.3V	Always
SPI3_SOUT	P1-96	O	Master data out; slave data in	3.3V	Always
SPI3_SCLK	P1-100	O	Master clock out; slave clock in	3.3V	Always
SPI3_PCS0	P1-97	O	Chip select 0	3.3V	Always
SPI3_PCS1	P2-93	O	Chip select 1	3.3V	Always

NOTE: SPI3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 42 SPI4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SPI4_SIN	P1-34 P1-85	I	Master data in; slave data out	3.3V	Always
SPI4_SOUT	P1-28	O	Master data out; slave data in	3.3V	Always
SPI4_SCLK	P1-26	O	Master clock out; slave clock in	3.3V	Always
SPI4_PCS0	P1-32	O	Chip select 0	3.3V	Always
SPI4_PCS1	P1-30	O	Chip select 1	3.3V	Always
SPI4_PCS2	P1-36 P2-90	O	Chip select 2	3.3V	Always

NOTE: SPI4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 43 SPI5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SPI5_SIN	P1-34	I	Master data in; slave data out	3.3V	Always
SPI5_SOUT	P1-28	O	Master data out; slave data in	3.3V	Always
SPI5_SCLK	P1-26	O	Master clock out; slave clock in	3.3V	Always
SPI5_PCS0	P1-32	O	Chip select 0	3.3V	Always
SPI5_PCS1	P1-49	O	Chip select 1	3.3V	Always

NOTE: SPI5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 44 SPI6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SPI6_SIN	P1-21	I	Master data in; slave data out	3.3V	Only w/o 'WB' option
SPI6_SOUT	P1-89	O	Master data out; slave data in	3.3V	Only w/o 'WB' option
SPI6_SCLK	P1-87	O	Master clock out; slave clock in	3.3V	Only w/o 'WB' option
SPI6_PCS0	P1-61	O	Chip select 0	3.3V	Only w/o 'WB' option

NOTE: SPI6 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 45 SPI7 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SPI7_SIN	P2-89	I	Master data in; slave data out	3.3V	Always
SPI7_SOUT	P2-95	O	Master data out; slave data in	3.3V	Always
SPI7_SCLK	P2-93	O	Master clock out; slave clock in	3.3V	Always
SPI7_PCS0	P2-91	O	Chip select 0	3.3V	Always
SPI7_PCS1	P1-33	O	Chip select 1	3.3V	Always

NOTE: SPI7 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 46 SPI8 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
SPI8_SIN	P1-37	I	Master data in; slave data out	3.3V	Always
SPI8_SOUT	P1-72	O	Master data out; slave data in	3.3V	Always
SPI8_SCLK	P1-19	O	Master clock out; slave clock in	3.3V	Always
SPI8_PCS0	P1-35	O	Chip select 0	3.3V	Always
SPI8_PCS1	P1-38	O	Chip select 1	3.3V	Always

NOTE: SPI8 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.13 I2C

UCM-iMX95 features up-to seven I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Multi-master operation

Please refer to the i.MX95 Reference manual for additional details.

The tables below summarize the I2C interface signals.

Table 47 I2C3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
I2C3_SCL	P1-94	O	I2C serial clock line	3.3V	Always
	P1-21				Only w/o 'WB' option
I2C3_SDA	P1-91	IO	I2C serial data line	3.3V	Always
	P1-61				Only w/o 'WB' option

NOTE: I2C3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 48 I2C4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
I2C4_SCL	P1-53	O	I2C serial clock line	3.3V	Always
	P1-87				Only w/o 'WB' option
I2C4_SDA	P1-51	IO	I2C serial data line	3.3V	Always
	P1-89				Only w/o 'WB' option

NOTE: I2C4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 49 I2C5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
I2C5_SCL	P1-81	O	I2C serial clock line	3.3V	Always
	P1-21				Only w/o 'WB' option
I2C5_SDA	P1-79	IO	I2C serial data line	3.3V	Always
	P1-61				Only w/o 'WB' option

NOTE: I2C5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 50 I2C6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
I2C6_SCL	P2-89	O	I2C serial clock line	3.3V	Always
	P1-87				Only w/o 'WB' option
I2C6_SDA	P2-91	IO	I2C serial data line	3.3V	Always
	P1-89				Only w/o 'WB' option

NOTE: I2C6 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 51 I2C7 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
I2C7_SCL	P1-99	O	I2C serial clock line	3.3V	Always
	P2-93				
I2C7_SDA	P1-97	IO	I2C serial data line	3.3V	Always
	P2-95				

NOTE: I2C7 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 52 I2C8 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
I2C8_SCL	P1-37	O	I2C serial clock line	3.3V	Always
	P1-100				
I2C8_SDA	P1-35	IO	I2C serial data line	3.3V	Always
	P1-96				

NOTE: I2C8 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.14 I3C

UCM-iMX95 supports one I3C bus interface.

Please refer to the i.MX95 Reference manual for additional details.

The tables below summarize the I3C interface signals.

Table 53 I3C2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
I3C2_SCL	P2-92	O	Serial clock line	SD2	Always
I3C2_SDA	P2-96	IO	Serial data line	SD2	Always

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
I3C2_PUR	P2-100	O	Pull up resistance. There is internal pull-up resistance on SDA, which is controlled by the I3C controller. If the internal pullup is not enough, PUR can be used to control an external pull-up resistance on SDA actively.	SD2	Always

NOTE: I3C signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pins denoted "SD2" can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL.

4.15 Timer/Pulse Width Modulation

i.MX95 supports five multi-channel timer modules (TPM) that can be used for electric motor control and power management. The timer modules support:

- Input capture
- Output comparison
- Generation of PWM signals

Please refer to the i.MX95 Reference manual for additional details.

The table below summarizes the PDM interface signals.

Table 54 TPM1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
TPM1_EXTCLK	P3-4	I	External clock	3.3V	Always
TPM1_CH0	P1-76	IO	Channel 0 I/O pin	3.3V	Always
TPM1_CH1	P1-74	IO	Channel 1 I/O pin	3.3V	Always
TPM1_CH2	P1-84	IO	Channel 2 I/O pin	3.3V	Always
TPM1_CH3	P1-86	IO	Channel 3 I/O pin	3.3V	Always

Table 55 TPM3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
TPM3_EXTCLK	P1-99	I	External clock	3.3V	Always
TPM3_CH0	P2-91	IO	Channel 0 I/O pin	3.3V	Always
TPM3_CH1	P1-28	IO	Channel 1 I/O pin	3.3V	Always
TPM3_CH2	P1-35	IO	Channel 2 I/O pin	3.3V	Always

Table 56 TPM4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
TPM4_EXTCLK	P1-96	I	External clock	3.3V	Always
TPM4_CH0	P2-89	IO	Channel 0 I/O pin	3.3V	Always
TPM4_CH1	P1-26	IO	Channel 1 I/O pin	3.3V	Always
TPM4_CH2	P1-37	IO	Channel 2 I/O pin	3.3V	Always

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
TPM4_CH3	P1-33	IO	Channel 3 I/O pin	3.3V	Always

Table 57 TPM5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
TPM5_EXTCLK	P1-100	I	External clock	3.3V	Always
TPM5_CH0	P2-95	IO	Channel 0 I/O pin	3.3V	Always
TPM5_CH1	P1-79	IO	Channel 1 I/O pin	3.3V	Always
TPM5_CH2	P1-32	IO	Channel 2 I/O pin	3.3V	Always
TPM5_CH3	P1-38	IO	Channel 3 I/O pin	3.3V	Always

Table 58 TPM6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
TPM6_EXTCLK	P1-79	I	External clock	3.3V	Always
TPM6_CH0	P1-97	IO	Channel 0 I/O pin	3.3V	Always
TPM6_CH1	P1-81	IO	Channel 1 I/O pin	3.3V	Always
TPM6_CH2	P1-34	IO	Channel 2 I/O pin	3.3V	Always
TPM6_CH3	P1-49	IO	Channel 3 I/O pin	3.3V	Always

NOTE: TPM signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.16 ADC

UCM-iMX95 features an 8-channel 12-bit ADC implemented in the i.MX95 SoC.

Please refer to the i.MX95 Reference manual for additional details.

The following table summarizes ADC signals.

Table 59 ADC Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
ADC_IN0	P3-1	AI	ADC input channel 0	1.8V	Always
ADC_IN1	P3-3	AI	ADC input channel 1	1.8V	Always
ADC_IN2	P3-5	AI	ADC input channel 2	1.8V	Always
ADC_IN3	P3-7	AI	ADC input channel 3	1.8V	Always
ADC_IN4	P3-11	AI	ADC input channel 4	1.8V	Always
ADC_IN5	P3-13	AI	ADC input channel 5	1.8V	Always
ADC_IN6	P3-15	AI	ADC input channel 6	1.8V	Always
ADC_IN7	P3-17	AI	ADC input channel 7	1.8V	Always

4.17 JTAG

UCM-iMX95 enables access to the i.MX95 JTAG port through the carrier board interface.

Please refer to the i.MX95 Reference manual for additional details.

The table below summarizes the JTAG interface signals.

Table 60 JTAG Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
JTAG_TCK	P1-73	I	Test clock	1.8V	Always
JTAG_TDI	P1-71	I	Test data in	1.8V	Always
JTAG_TDO	P1-67	O	Test data out	1.8V	Always
JTAG_TMS	P1-65	I	Test mode select	1.8V	Always

NOTE: JTAG signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.18 GPIO

Up-to 94 of the i.MX95 general purpose input/output (GPIO) signals are available through the UCM-iMX95 carrier board interface. In addition, GPIO signals can produce interrupts.

Please refer to the i.MX95 Reference manual for additional details.

NOTE: GPIO signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Signals that belong to "SD2" domain can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL.

NOTE: When the SOM is assembled with the "E" configuration option (on-board PHY), signals that belong to "ENET" domain operate at 3.3V voltage levels. When the SOM is assembled without the "E" configuration option, voltage level of "ENET" signals is controlled by EXT_ENET pin (P1-55).

The following table summarizes the GPIO interface signals.

Table 61 GPIO Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
GPIO2_IO[0]	P1-61	IO	General-purpose input/output	3.3V	Only w/o 'WB' option
GPIO2_IO[1]	P1-21	IO	General-purpose input/output	3.3V	Only w/o 'WB' option
GPIO2_IO[2]	P1-89	IO	General-purpose input/output	3.3V	Only w/o 'WB' option
GPIO2_IO[3]	P1-87	IO	General-purpose input/output	3.3V	Only w/o 'WB' option
GPIO2_IO[4]	P2-91	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[5]	P2-89	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[6]	P2-95	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[7]	P2-93	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[8]	P1-97	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[9]	P1-99	IO	General-purpose input/output	3.3V	Always

GPIO2_IO[10]	P1-96	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[11]	P1-100	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[12]	P1-35	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[13]	P1-37	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[14]	P1-72	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[15]	P1-19	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[16]	P1-36	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[17]	P1-30	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[18]	P1-32	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[19]	P1-34	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[20]	P1-28	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[21]	P1-26	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[22]	P1-79	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[23]	P1-81	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[25]	P1-33	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[26]	P1-38	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[27]	P1-49	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[28]	P1-91	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[29]	P1-94	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[30]	P1-51	IO	General-purpose input/output	3.3V	Always
GPIO2_IO[31]	P1-53	IO	General-purpose input/output	3.3V	Always
GPIO5_IO[12]	P2-90	IO	General-purpose input/output	3.3V	Always
GPIO5_IO[15]	P1-85	IO	General-purpose input/output	3.3V	Always
GPIO3_IO[27]	P3-21	IO	General-purpose input/output	1.8V	Always
GPIO4_IO[28]	P2-49	IO	General-purpose input/output	1.8V	Always
GPIO4_IO[29]	P2-52	IO	General-purpose input/output	1.8V	Always
GPIO3_IO[28]	P1-71	IO	General-purpose input/output	1.8V	Always
GPIO3_IO[29]	P1-65	IO	General-purpose input/output	1.8V	Always
GPIO3_IO[30]	P1-73	IO	General-purpose input/output	1.8V	Always
GPIO3_IO[31]	P1-67	IO	General-purpose input/output	1.8V	Always
GPIO4_IO[0]	P2-68	IO	General-purpose input/output	ENET	Always
GPIO4_IO[1]	P2-70	IO	General-purpose input/output	ENET	Always
GPIO4_IO[14]	P2-76	IO	General-purpose input/output	ENET	Always
GPIO4_IO[15]	P2-60	IO	General-purpose input/output	ENET	Always
GPIO4_IO[16]	P2-65	IO	General-purpose input/output	ENET	Always
GPIO4_IO[17]	P2-63	IO	General-purpose input/output	ENET	Always
GPIO4_IO[18]	P2-61	IO	General-purpose input/output	ENET	Always
GPIO4_IO[19]	P2-59	IO	General-purpose input/output	ENET	Always
GPIO4_IO[20]	P2-67	IO	General-purpose input/output	ENET	Always
GPIO4_IO[21]	P2-69	IO	General-purpose input/output	ENET	Always
GPIO4_IO[22]	P2-53	IO	General-purpose input/output	ENET	Always
GPIO4_IO[23]	P2-55	IO	General-purpose input/output	ENET	Always
GPIO4_IO[24]	P2-41	IO	General-purpose input/output	ENET	Always
GPIO4_IO[25]	P2-43	IO	General-purpose input/output	ENET	Always
GPIO4_IO[26]	P2-45	IO	General-purpose input/output	ENET	Always
GPIO4_IO[27]	P2-47	IO	General-purpose input/output	ENET	Always
GPIO3_IO[19]	P2-62	IO	General-purpose input/output	1.8V	Always

GPIO3_IO[20]	P1-75	IO	General-purpose input/output	1.8V	Only w/o 'WB' option
GPIO3_IO[21]	P1-77	IO	General-purpose input/output	1.8V	Only w/o 'WB' option
GPIO3_IO[22]	P1-59	IO	General-purpose input/output	1.8V	Only w/o 'WB' option
GPIO3_IO[23]	P1-60	IO	General-purpose input/output	1.8V	Only w/o 'WB' option
GPIO3_IO[24]	P1-62	IO	General-purpose input/output	1.8V	Only w/o 'WB' option
GPIO3_IO[25]	P1-63	IO	General-purpose input/output	1.8V	Only w/o 'WB' option
GPIO5_IO[0]	P3-22	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[1]	P3-24	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[2]	P3-28	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[3]	P3-30	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[4]	P3-32	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[5]	P3-36	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[6]	P3-38	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[7]	P3-40	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[8]	P3-14	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[9]	P3-10	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[10]	P3-20	IO	General-purpose input/output	1.8V	Always
GPIO5_IO[11]	P3-16	IO	General-purpose input/output	1.8V	Always
GPIO3_IO[0]	P2-92	IO	General-purpose input/output	SD2	Always
GPIO3_IO[1]	P2-96	IO	General-purpose input/output	SD2	Always
GPIO3_IO[2]	P2-100	IO	General-purpose input/output	SD2	Always
GPIO3_IO[3]	P2-97	IO	General-purpose input/output	SD2	Always
GPIO3_IO[4]	P2-99	IO	General-purpose input/output	SD2	Always
GPIO3_IO[5]	P2-94	IO	General-purpose input/output	SD2	Always
GPIO3_IO[6]	P2-98	IO	General-purpose input/output	SD2	Always
GPIO3_IO[7]	P2-51	IO	General-purpose input/output	SD2	Always
GPIO1_IO[4]	P1-76	IO	General-purpose input/output	3.3V	Always
GPIO1_IO[5]	P1-74	IO	General-purpose input/output	3.3V	Always
GPIO1_IO[6]	P1-84	IO	General-purpose input/output	3.3V	Always
GPIO1_IO[7]	P1-86	IO	General-purpose input/output	3.3V	Always
GPIO1_IO[8]	P3-2	IO	General-purpose input/output	3.3V	Always
GPIO1_IO[9]	P3-4	IO	General-purpose input/output	3.3V	Always
GPIO1_IO[10]	P3-6	IO	General-purpose input/output	3.3V	Always
GPIO1_IO[11]	P1-95	IO	General-purpose input/output	3.3V	Always
GPIO1_IO[12]	P1-70	IO	General-purpose input/output	3.3V	Always
GPIO1_IO[13]	P1-92	IO	General-purpose input/output	3.3V	Always
GPIO1_IO[14]	P1-98	IO	General-purpose input/output	3.3V	Always

5 SYSTEM LOGIC

5.1 Power Supply

Table 62 Power signals

Signal Name	Connector #	Pin#	Type	Description
V_SOM	P1	11, 27, 43, 57, 69, 83	P	Main power supply. Connect to a regulated DC supply or Li-Ion battery
	P2	9, 19, 29, 39, 57, 71, 87		
VCC_RTC	P1	93	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. If RTC back-up is not required, connect this pin to GND.
EXT_ENET	P1	55	P	ENET domain power supply input. When the SOM is assembled with the "E" configuration option (on-board PHY), signals that belong to "ENET" domain operate at 3.3V voltage levels. When the SOM is assembled without the "E" configuration option, external power MUST be supplied from the carrier-board via EXT_ENET pin.
GND	P1	4, 10, 20, 40, 54, 64, 78, 88	P	Common ground
	P2	10, 16, 22, 28, 34, 40, 46, 54, 72, 82		
	P3	8, 9, 12, 18, 19, 23, 26, 29, 34, 35		

5.2 I/O Voltage Domains

UCM-iMX95 utilizes four separate I/O voltage domains that are used to power different I/O modules of the i.MX95 SoC.

Table 63 Power signals

I/O Voltage Domain	Description	Default Voltage	Control
3.3V	Main 3.3V	3.3V	N/A
1.8V	Main 1.8V	1.8V	N/A
SD2	SD2 interface power supply. Powered with PMIC LDO2.	3.3V	SD2_VSEL (SoC pin GPIO3_IO19)
ENET	RGMII interfaces power supply. When "E" option is present this domain is supplied from on-board +3.3V. When UCM-iMX95 is assembled without "E" option this domain must be supplied from carrier-board via pin +EXT_ENET.	With "E" option: 3.3V Without "E" option: EXT_ENET (P1-55)	N/A

5.3 System and Miscellaneous Signals

5.3.1 Power management

UCM-iMX95 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX95 SoC. The logic that controls both signals is supplied by the i.MX95 SoC BBSM power rail.

The PMIC_STBY output can be used to signal the carrier board power supply that UCM-iMX95 is in 'standby' or 'OFF' mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX95 Reference manual for additional details. The table below summarizes the external regulator control signals.

Table 64 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY	P1-66	O	When the processor enters SUSPEND mode, it will assert this signal.	Always available
PMIC_ON_REQ	P1-68	O	Active high power-up request output from i.MX95 SoC.	Always available
ONOFF	P2-64	I	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).	Always available

5.3.2 SD2 control

SD2_VSEL signal controls the voltage of the SD2 interface. By default there is an internal 1-4M ohm pull down resistor, and the voltage level is 3.3V. Changing the voltage level to 1.8V can be done by pulling SD2_VSEL up using a 10-100K ohm pull up resistor to 1.8/3.3V. Please refer to the i.MX95 Reference manual for additional details.

Table 65 SD2 control

Signal Name	Pin #	Type	Description	Availability
SD2_VSEL	P1-62	I	SD2 voltage control	Always

5.4 Reset

COLD_RESET_IN signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on UCM-iMX95. Please refer to the i.MX95 Reference manual for additional details.

Table 66 Reset signals

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	P1-2	I	Active Low cold reset input signal. Should be used as main system reset	Always
POR_B_3V3	P2-66	I	CPU power on reset input pin, active low	Always

5.5 Boot Sequence

UCM-iMX95 boot sequence defines which interface/media is used by UCM-iMX95 to load and execute the initial software (such as SPL or/and U-boot). UCM-iMX95 can load initial software from the following interfaces/media:

- On-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD card using the SD2 interface
- Serial Download boot using USB1 interface

UCM-iMX95 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of three different boot sequences are supported by UCM-iMX95:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternative sequence: designed to allow recovery from an external bootable SD card in case of data corruption of the on-board primary boot device. Using the alternate sequence allows UCM-iMX95 to boot bypassing the onboard eMMC.
- Serial download mode: provides a means to download a program image to the i.MX95 system-on-chip over USB serial connection

Logic values of boot selections signals define which of the supported boot sequences is used by the system.

Table 67 Boot selection signals

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT#	P1-90	I	Active low alternate boot sequence select input. Leave floating or tie high for standard boot sequence	Always available
SDP_BOOT#	P2-88	I	Active low alternate boot sequence select input. Leave floating or tie high for standard boot sequence	Always available

Table 68 UCM-iMX95 boot sequences

Mode	ALT_BOOT#	SDP_BOOT#	Booting sequence
Standard	High or floating	High or floating	Onboard eMMC (primary boot storage)
Alternative	Low	Low, high or floating	SD card on SD2 interface
SDP mode	High or floating	Low	Serial Downloader on USB1

5.6 Signal Multiplexing Characteristics

Up to 94 of the UCM-iMX95 carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the UCM-iMX95 CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 8 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of UCM-iMX95 pins are derived from the i.MX95 SoC control module.

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time. Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

NOTE: Signals that belong to "SD2" domain can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL.

NOTE: When the SOM is assembled with the "E" configuration option (on-board PHY), signals that belong to "ENET" domain operate at 3.3V voltage levels. When the SOM is assembled without the "E" configuration option, voltage level of "ENET" signals is controlled by EXT_ENET pin (P1-55).

Table 69 Multifunctional Signals

Pin #	SoC Pin Name	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	Domain	Pin Availability
P1-61	GPIO_IO00	GPIO2_IO[0]	I2C3_SDA			SPI6_PCS0	UART5_TX	I2C5_SDA		3.3V	Only w/o 'WB'
P1-21	GPIO_IO01	GPIO2_IO[1]	I2C3_SCL			SPI6_SIN	UART5_RX	I2C5_SCL		3.3V	Only w/o 'WB'
P1-89	GPIO_IO02	GPIO2_IO[2]	I2C4_SDA			SPI6_SOUT	UART5_CTS_B	I2C6_SDA		3.3V	Only w/o 'WB'
P1-87	GPIO_IO03	GPIO2_IO[3]	I2C4_SCL			SPI6_SCK	UART5_RTS_B	I2C6_SCL		3.3V	Only w/o 'WB'
P2-91	GPIO_IO04	GPIO2_IO[4]	TPM3_CH0	PDM_CLK	CAN4_TX	SPI7_PCS0	UART6_TX	I2C6_SDA		3.3V	Always
P2-89	GPIO_IO05	GPIO2_IO[5]	TPM4_CH0	PDM_BIT_STREAM[0]	CAN4_RX	SPI7_SIN	UART6_RX	I2C6_SCL		3.3V	Always
P2-95	GPIO_IO06	GPIO2_IO[6]	TPM5_CH0	PDM_BIT_STREAM[1]		SPI7_SOUT	UART6_CTS_B	I2C7_SDA		3.3V	Always
P2-93	GPIO_IO07	GPIO2_IO[7]	SPI3_PCS1			SPI7_SCK	UART6_RTS_B	I2C7_SCL		3.3V	Always
P1-97	GPIO_IO08	GPIO2_IO[8]	SPI3_PCS0			TPM6_CH0	UART7_TX	I2C7_SDA		3.3V	Always
P1-99	GPIO_IO09	GPIO2_IO[9]	SPI3_SIN			TPM3_EXTCLK	UART7_RX	I2C7_SCL		3.3V	Always
P1-96	GPIO_IO10	GPIO2_IO[10]	SPI3_SOUT			TPM4_EXTCLK	UART7_CTS_B	I2C8_SDA		3.3V	Always

P1-100	GPIO_IO11	GPIO2_IO[11]	SPI3_SCK			TPM5_EXTCLK	UART7_RTS_B	I2C8_SCL		3.3V	Always
P1-35	GPIO_IO12	GPIO2_IO[12]	TPM3_CH2	PDM_BIT_STREAM[2]		SPI8_PCS0	UART8_TX	I2C8_SDA	SAI3_RX_SYNC	3.3V	Always
P1-37	GPIO_IO13	GPIO2_IO[13]	TPM4_CH2	PDM_BIT_STREAM[3]		SPI8_SIN	UART8_RX	I2C8_SCL		3.3V	Always
P1-72	GPIO_IO14	GPIO2_IO[14]	UART3_TX			SPI8_SOUT	UART8_CTS_B	UART4_TX		3.3V	Always
P1-19	GPIO_IO15	GPIO2_IO[15]	UART3_RX			SPI8_SCK	UART8_RTS_B	UART4_RX		3.3V	Always
P1-36	GPIO_IO16	GPIO2_IO[16]	SAI3_TX_BCLK	PDM_BIT_STREAM[2]		UART3_CTS_B	SPI4_PCS2	UART4_CTS		3.3V	Always
P1-30	GPIO_IO17	GPIO2_IO[17]	SAI3_MCLK			UART3_RTS_B	SPI4_PCS1	UART4_RTS		3.3V	Always
P1-32	GPIO_IO18	GPIO2_IO[18]	SAI3_RX_BCLK			SPI5_PCS0	SPI4_PCS0	TPM5_CH2		3.3V	Always
P1-34	GPIO_IO19	GPIO2_IO[19]	SAI3_RX_SYNC	PDM_BIT_STREAM[3]		SPI5_SIN	SPI4_SIN	TPM6_CH2	SAI3_TX_ DATA[0]	3.3V	Always
P1-28	GPIO_IO20	GPIO2_IO[20]	SAI3_RX_DATA[0]	PDM_BIT_STREAM[0]		SPI5_SOUT	SPI4_SOUT	TPM3_CH1		3.3V	Always
P1-26	GPIO_IO21	GPIO2_IO[21]	SAI3_TX_DATA[0]	PDM_CLK		SPI5_SCK	SPI4_SCK	TPM4_CH1	SAI3_RX_BCLK	3.3V	Always
P1-79	GPIO_IO22	GPIO2_IO[22]	USDHC3_CLK	SPDIF1_IN	CAN5_TX	TPM5_CH1	TPM6_EXTCLK	I2C5_SDA		3.3V	Always
P1-81	GPIO_IO23	GPIO2_IO[23]	USDHC3_CMD	SPDIF1_OUT	CAN5_RX	TPM6_CH1		I2C5_SCL		3.3V	Always
P1-33	GPIO_IO25	GPIO2_IO[25]	USDHC3_DATA1	CAN2_TX		TPM4_CH3	JTAG_TCLK	SPI7_PCS1		3.3V	Always
P1-38	GPIO_IO26	GPIO2_IO[26]	USDHC3_DATA2	PDM_BIT_STREAM[1]		TPM5_CH3	JTAG_TDI	SPI8_PCS1	SAI3_TX_SYNC	3.3V	Always
P1-49	GPIO_IO27	GPIO2_IO[27]	USDHC3_DATA3	CAN2_RX		TPM6_CH3	JTAG_TMS	SPI5_PCS1		3.3V	Always
P1-91	GPIO_IO28	GPIO2_IO[28]	I2C3_SDA	CAN3_TX						3.3V	Always
P1-94	GPIO_IO29	GPIO2_IO[29]	I2C3_SCL	CAN3_RX						3.3V	Always
P1-51	GPIO_IO30	GPIO2_IO[30]	I2C4_SDA	CAN5_TX						3.3V	Always
P1-53	GPIO_IO31	GPIO2_IO[31]	I2C4_SCL	CAN5_RX						3.3V	Always
P2-90	GPIO_IO32	GPIO5_IO[12]	PCIE1_CLKREQ_B	UART6_TX		SPI4_PCS2				3.3V	Always
P1-85	GPIO_IO35	GPIO5_IO[15]	PCIE2_CLKREQ_B	UART6_RTS_B		SPI4_SIN				3.3V	Always
P3-21	CCM_CLKO2	CLKO2	TMR_1588_PP1				GPIO3_IO[27]			1.8V	Always
P2-49	CCM_CLKO3	CLKO3	TMR_1588_TRIG2	CAN3_TX			GPIO4_IO[28]			1.8V	Always
P2-52	CCM_CLKO4	CLKO4	TMR_1588_PP2	CAN3_RX			GPIO4_IO[29]			1.8V	Always
P1-71	JTAG_TDI	JTAG_TDI	MQS2_LEFT	TMR_1588_ALARM1	CAN2_TX		GPIO3_IO[28]	UART5_RX		1.8V	Always
P1-65	JTAG_TMS	JTAG_TMS		CAN4_TX			GPIO3_IO[29]	UART5_RTS		1.8V	Always
P1-73	JTAG_TCLK	JTAG_TCLK		CAN4_RX			GPIO3_IO[30]	UART5_CTS		1.8V	Always

P1-67	JTAG_TDO	JTAG_TDO	MQS2_RIGHT	TMR_1588_ALARM2	CAN2_RX		GPIO3_IO[31]	UART5_TX		1.8V	Always
P2-68	ENET1_MDC	MDC	UART3_DCB_B	I3C2_SCL	USB1_OTG_ID		GPIO4_IO[0]			ENET	Always
P2-70	ENET1_MDIO	MDIO	UART3_RIN_B	I3C2_SDA	USB1_OTG_PWR		GPIO4_IO[1]			ENET	Always
P2-76	ENET2_MDC	MDC	UART4_DCB_B	SAI2_RX_SYNC			GPIO4_IO[14]			ENET	Always
P2-60	ENET2_MDIO	MDIO	UART4_RIN_B	SAI2_RX_BCLK			GPIO4_IO[15]			ENET	Always
P2-65	ENET2_TD3	RGMII_TXD[3]		SAI2_RX_DATA[0]			GPIO4_IO[16]			ENET	Always
P2-63	ENET2_TD2	RGMII_TXD[2]		SAI2_RX_DATA[1]	SAI4_TX_SYNC		GPIO4_IO[17]			ENET	Always
P2-61	ENET2_TD1	RGMII_TXD[1]	UART4_RTS_B	SAI2_RX_DATA[2]	SAI4_TX_BCLK		GPIO4_IO[18]	RMII_TXD[1]		ENET	Always
P2-59	ENET2_TD0	RGMII_TXD[0]	UART4_TX	SAI2_RX_DATA[3]	SAI4_TX_DATA[0]		GPIO4_IO[19]	RMII_TXD[0]		ENET	Always
P2-67	ENET2_TX_CTL	RGMII_TX_CTL	UART4_DTR_B	SAI2_TX_SYNC	RMII_TX_EN		GPIO4_IO[20]			ENET	Always
P2-69	ENET2_TXC	RGMII_TX_CLK		SAI2_TX_BCLK			GPIO4_IO[21]			ENET	Always
P2-53	ENET2_RX_CTL	RGMII_RX_CTL	UART4_DSR_B	SAI2_TX_DATA[0]			GPIO4_IO[22]	RMII_CRS_DV		ENET	Always
P2-55	ENET2_RXC	RGMII_RX_CLK	RMII_RX_ER	SAI2_TX_DATA[1]	SAI4_RX_SYNC		GPIO4_IO[23]			ENET	Always
P2-41	ENET2_RD0	RGMII_RXD[0]	UART4_RX	SAI2_TX_DATA[2]	SAI4_RX_BCLK		GPIO4_IO[24]	RMII_RXD[0]		ENET	Always
P2-43	ENET2_RD1	RGMII_RXD[1]	SPDIF1_IN	SAI2_TX_DATA[3]	SAI4_RX_DATA[0]		GPIO4_IO[25]	RMII_RXD[1]		ENET	Always
P2-45	ENET2_RD2	RGMII_RXD[2]	UART4_CTS_B	SAI2_MCLK	MQS2_RIGHT		GPIO4_IO[26]	RMII_RX_ER		ENET	Always
P2-47	ENET2_RD3	RGMII_RXD[3]	SPDIF1_OUT	SPDIF1_IN	MQS2_LEFT		GPIO4_IO[27]			ENET	Always
P2-62	SD2_VSELECT	SD2_VSELECT	USDHC2_WP	lptmr2_ALT3			GPIO3_IO[19]			1.8V	Always
P1-75	SD3_CLK	SD3_CLK	SPI_A_SCLK	SAI5_TX_DATA[1]	SAI5_RX_DATA[0]		GPIO3_IO[20]	XSPI_SLV_CLK		1.8V	Only w/o 'WB'
P1-77	SD3_CMD	SD3_CMD	SPI_A_SS0_B	SAI5_TX_DATA[2]	SAI5_RX_SYNC		GPIO3_IO[21]	XSPI_SLV_CS		1.8V	Only w/o 'WB'
P1-59	SD3_DATA0	SD3_DATA0	SPI_A_DATA[0]	SAI5_TX_DATA[3]	SAI5_RX_BCLK		GPIO3_IO[22]	XSPI_SLV_DATA[0]		1.8V	Only w/o 'WB'
P1-60	SD3_DATA1	SD3_DATA1	SPI_A_DATA[1]	SAI5_RX_DATA[1]	SAI5_TX_DATA[0]		GPIO3_IO[23]	XSPI_SLV_DATA[1]		1.8V	Only w/o 'WB'
P1-62	SD3_DATA2	SD3_DATA2	SPI_A_DATA[2]	SAI5_RX_DATA[2]	SAI5_TX_SYNC		GPIO3_IO[24]	XSPI_SLV_DATA[2]		1.8V	Only w/o 'WB'
P1-63	SD3_DATA3	SD3_DATA3	SPI_A_DATA[3]	SAI5_RX_DATA[3]	SAI5_TX_BCLK		GPIO3_IO[25]	XSPI_SLV_DATA[3]		1.8V	Only w/o 'WB'
P3-22	XSPI1_DATA0	SPI_A_DATA[0]	SAI2_TX_DATA[4]	SAI4_TX_BCLK	SAI4_RX_DATA[1]	xSPI_slv_DATA[0]	GPIO5_IO[0]			1.8V	Always
P3-24	XSPI1_DATA1	SPI_A_DATA[1]	SAI2_TX_DATA[5]	SAI4_TX_SYNC	SAI4_TX_DATA[1]	xSPI_slv_DATA[1]	GPIO5_IO[1]			1.8V	Always
P3-28	XSPI1_DATA2	SPI_A_DATA[2]	SAI2_TX_DATA[6]	SAI4_TX_DATA[0]		xSPI_slv_DATA[2]	GPIO5_IO[2]			1.8V	Always
P3-30	XSPI1_DATA3	SPI_A_DATA[3]	SAI2_TX_DATA[7]	SAI4_RX_DATA[0]		xSPI_slv_DATA[3]	GPIO5_IO[3]			1.8V	Always
P3-32	XSPI1_DATA4	SPI_A_DATA[4]	SAI5_TX_DATA[0]	SAI5_RX_DATA[1]		xSPI_slv_DATA[4]	GPIO5_IO[4]			1.8V	Always

P3-36	XSPI1_DATA5	SPI_A_DATA[5]	SAI5_TX_SYNC	SAI5_RX_DATA[2]	SAI2_RX_DATA[6]	xSPI_slv_DATA[5]	GPIO5_IO[5]			1.8V	Always
P3-38	XSPI1_DATA6	SPI_A_DATA[6]	SAI5_TX_BCLK	SAI5_RX_DATA[3]	SAI2_RX_DATA[7]	xSPI_slv_DATA[6]	GPIO5_IO[6]			1.8V	Always
P3-40	XSPI1_DATA7	SPI_A_DATA[7]	SAI5_RX_DATA[0]	SAI5_TX_DATA[1]		xSPI_slv_DATA[7]	GPIO5_IO[7]			1.8V	Always
P3-14	XSPI1_DQS	SPI_A_DQS	SAI5_RX_SYNC	SAI5_TX_DATA[2]	SAI2_RX_DATA[6]	xSPI_slv_DQS	GPIO5_IO[8]			1.8V	Always
P3-10	XSPI1_SCLK	SPI_A_SCLK	SAI2_RX_DATA[4]	SAI4_RX_SYNC	earc_hpd	xSPI_slv_CLK	GPIO5_IO[9]			1.8V	Always
P3-20	XSPI1_SS0_B	SPI_A_SS0_B	SAI2_RX_DATA[5]	SAI4_RX_BCLK	earc_cec	xSPI_slv_CS	GPIO5_IO[10]			1.8V	Always
P3-16	XSPI1_SS1_B	SPI_A_SS1_B	SAI5_RX_BCLK	SAI5_TX_DATA[3]	SAI2_RX_DATA[7]		GPIO5_IO[11]			1.8V	Always
P2-92	SD2_CD_B	SD2_CD_B	TMR_1588_TRIG1	I3C2_SCL			GPIO3_IO[0]			SD2	Always
P2-96	SD2_CLK	SD2_CLK	TMR_1588_PP1	I3C2_SDA			GPIO3_IO[1]			SD2	Always
P2-100	SD2_CMD	SD2_CMD	TMR_1588_TRIG2	I3C2_PUR	I3C2_PUR_B		GPIO3_IO[2]			SD2	Always
P2-97	SD2_DATA0	SD2_DATA0	TMR_1588_PP2	CAN2_TX			GPIO3_IO[3]			SD2	Always
P2-99	SD2_DATA1	SD2_DATA1	TMR_1588_CLK	CAN2_RX			GPIO3_IO[4]			SD2	Always
P2-94	SD2_DATA2	SD2_DATA2	TMR_1588_PP3	MQS2_RIGHT			GPIO3_IO[5]			SD2	Always
P2-98	SD2_DATA3	SD2_DATA3		MQS2_LEFT	TMR_1588_ALARM1		GPIO3_IO[6]			SD2	Always
P2-51	SD2_RESET_B	SD2_RESET_B			TMR_1588_GCLK		GPIO3_IO[7]			SD2	Always
P1-76	UART1_RXD	UART1_RX		SPI2_SIN	TPM1_CH0	vpu_UART_RX	GPIO1_IO[4]			3.3V	Always
P1-74	UART1_TXD	UART1_TX		SPI2_PCS0	TPM1_CH1	vpu_UART_TX	GPIO1_IO[5]/ BOOT_MODE[0]			3.3V	Output only
P1-84	UART2_RXD	UART2_RX	UART1_CTS_B	SPI2_SOUT	TPM1_CH2	SAI1_MCLK	GPIO1_IO[6]			3.3V	Always
P1-86	UART2_TXD	UART2_TX	UART1_RTS_B	SPI2_SCK	TPM1_CH3		GPIO1_IO[7]/ BOOT_MODE[1]			3.3V	Output only
P3-2	PDM_CLK	PDM_CLK	MQS1_LEFT			lptmr1_ALT1	GPIO1_IO[8]	CAN1_TX		3.3V	Always
P3-4	PDM_BIT_STREAM0	PDM_BIT_ STREAM[0]	MQS1_RIGHT	SPI1_PCS1	TPM1_EXTCLK	lptmr1_ALT2	GPIO1_IO[9]	CAN1_RX		3.3V	Always
P3-6	PDM_BIT_STREAM1	PDM_BIT_ STREAM[1]	m33_NMI	SPI2_PCS1	TPM2_EXTCLK	lptmr1_ALT3	GPIO1_IO[10]			3.3V	Always
P1-95	SAI1_TXFS	SAI1_TX_SYNC	SAI1_TX_DATA[1]	SPI1_PCS0	UART2_DTR_B	MQS1_LEFT	GPIO1_IO[11]/ BOOT_MODE[2]			3.3V	Output only
P1-70	SAI1_TXC	SAI1_TX_BCLK	UART2_CTS_B	SPI1_SIN	UART1_DSR_B	CAN1_RX	GPIO1_IO[12]			3.3V	Always
P1-92	SAI1_TXD0	SAI1_TX_DATA[0]	UART2_RTS_B	SPI1_SCK	UART1_DTR_B	CAN1_TX	GPIO1_IO[13]/ BOOT_MODE[3]			3.3V	Output only
P1-98	SAI1_RXD0	SAI1_RX_DATA[0]	SAI1_MCLK	SPI1_SOUT	UART2_DSR_B	MQS1_RIGHT	GPIO1_IO[14]			3.3V	Always

5.7 RTC

UCM-iMX95 features an on-board ultra-low-power RX8900CE real time clock (RTC). The RTC is connected to the i.MX95 SoC using I2C2 interface at address 0x32.

Back-up power supply is required in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about UCM-iMX95 RTC please refer to the RX8900CE datasheet.

5.8 LED

UCM-iMX95 features a single general purpose green LED controlled by PWR_LED (GPIO2_IO[24]) signal of the i.MX95. The LED is ON when PWR_LED is logic LOW.

5.9 Reserved Signals

The following UCM-iMX95 signals are reserved and must be left unconnected.

Table 70 Reserved Signals

Connector #	Pin#
P2	77

6 CARRIER BOARD INTERFACE

UCM-iMX95 carrier board interface uses two 100-pin and one 40-pin (optional) carrier board connectors. SoM pinout is detailed in the table below.

6.1 Connectors Pinout

Table 71 Connector P1

Pin #	UCM-iMX95 Signal Name	Ref.	Pin #	UCM-iMX95 Signal Name	Ref.
2	COLD_RESET_IN	5.3.2	1	USB2_VBUS	4.7
4	GND	5.1	3	USB2_DP	4.7
6	USB1_RX0_P	4.7	5	USB2_DN	4.7
8	USB1_RX0_N	4.7	7	USB1_RX1_P	4.7
10	GND	5.1	9	USB1_RX1_N	4.7
12	USB1_DP	4.7	11	V_SOM	5.1
14	USB1_DN	4.7	13	USB1_TX1_P	4.7
16	USB1_TX0_P	4.7	15	USB1_TX1_N	4.7
18	USB1_TX0_N	4.7	17	USB2_ID	4.7
20	GND	5.1	19	UART3_RX UART4_RXD UART8_RTS SPI8_SCLK GPIO2_IO[15]	4.10 4.10 4.10 4.12 4.19
22	USB1_ID	4.7	21	UART5_RX SPI6_SIN I2C3_SCL I2C5_SCL GPIO2_IO[1]	4.10 4.12 4.13 4.13 4.19
24	USB1_VBUS	4.7	23	PCIE_CLKOUT_P	4.5
26	SAI3_RX_BCLK SAI3_TX_DATA[0] PDM_CLK SPI4_SCLK SPI5_SCLK TPM4_CH1 GPIO2_IO[21]	4.3.2 4.3.2 4.3.4 04.12 4.12 04.15 4.19	25	PCIE_CLKOUT_N	4.5
28	SAI3_RX_DATA[0] PDM_BIT_STREAM0 SPI4_SOUT SPI5_SOUT TPM3_CH1 GPIO2_IO[20]	4.3.2 4.3.4 4.12 4.12 4.15 4.19	27	V_SOM	5.1
30	SAI3_MCLK UART3_RTS UART4_RTS SPI4_PCS1 GPIO2_IO[17]	4.3.2 4.10 4.10 4.12 4.19	29	PCIE2_CLKIN_P	4.5
32	SAI3_RX_BCLK SPI4_PCS0 SPI5_PCS0 TPM5_CH2 GPIO2_IO[18]	4.3.2 4.12 4.12 4.15 4.19	31	PCIE2_CLKIN_N	4.5
34	SAI3_RXFS SAI3_TX_DATA[0] PDM_ BIT_STREAM3 SPI4_SIN SPI5_SIN TPM6_CH2 GPIO2_IO[19]	4.3.2 4.3.2 4.3.4 4.12 4.12 4.15 4.19	33	CAN2_TX SPI7_PCS1 TPM4_CH3 SD3_DATA1 GPIO2_IO[25]	4.11 4.12 4.15 4.8 4.19

36	SAI3_TX_BCLK PDM_BIT_STREAM2 UART3_CTS UART4_CTS SPI4_PCS2 GPIO2_IO[16]	4.3.2 4.3.4 4.10 4.10 4.12 4.19		35	SAI3_RXFS PDM_BIT_STREAM2 UART8_TXD SPI8_PCS0 I2C8_SDA TPM3_CH2 GPIO2_IO[12]	4.3.2 4.3.4 4.10 4.12 4.13 4.15 4.19
38	SAI3_TXFS PDM_BIT_STREAM1 SD3_DATA2 SPI8_PCS1 TPM5_CH3 GPIO2_IO[26]	4.3.2 4.3.4 4.8 4.12 4.15 4.19		37	PDM_ BIT_STREAM3 UART8_RXD SPI8_SIN I2C8_SCL TPM4_CH2 GPIO2_IO[13]	4.3.4 4.10 4.12 4.13 4.15 4.19
40	GND	5.1		39	PCIE2_TX0_P	4.5
42	LVDS0_D0_P	4.1.2		41	PCIE2_TX0_N	4.5
44	LVDS0_D0_N	5.8		43	V_SOM	5.1
46	LVDS0_D1_P	5.8		45	PCIE2_RX0_P	4.5
48	LVDS0_D1_N	4.1.2		47	PCIE2_RX0_N	5.8
50	LVDS0_D2_P	4.1.2		49	SD3_DATA3 CAN2_RX SPI5_PCS1 TPM6_CH3 GPIO2_IO[27]	4.8 4.11 4.12 4.15 4.19
52	LVDS0_D2_N	4.1.2		51	CAN5_TX I2C4_SDA GPIO2_IO[30]	4.11 4.13 4.18
54	GND	5.1		53	CAN5_RX I2C4_SCL GPIO2_IO[31]	4.11 4.13 4.19
56	LVDS0_D3_P	4.1.2		55	EXT_ENET	4.4.3
58	LVDS0_D3_N	4.1.2		57	V_SOM	5.1
60	SAI5_RX_DATA[1] SAI5_TX_DATA[0] SD3_DATA1 XSPI_DATA1 GPIO3_IO[23]	4.3.2 4.3.2 4.8 4.9 4.19		59	SAI5_RX_BCLK SAI5_TX_DATA[3] SD3_DATA0 XSPI_DATA0 GPIO3_IO[22]	4.3.2 4.3.2 4.8 4.9 4.19
62	SAI5_RX_DATA[2] SAI5_TXFS SD3_DATA2 XSPI_DATA2 GPIO3_IO[24]	4.3.2 4.3.2 4.8 4.9 4.19		61	UART5_TX SPI6_PCS0 I2C3_SDA I2C5_SDA GPIO2_IO[0]	4.10 4.12 4.13 4.13 4.19
64	GND	5.1		63	SAI5_RX_DATA[3] SAI5_TX_BCLK SD3_DATA3 XSPI_DATA3 GPIO3_IO[25]	4.3.2 4.3.2 4.8 4.9 4.19
66	PMIC_STBY	5.3.1		65	UART5_RTS_B CAN4_TX JTAG_TMS GPIO3_IO[29]	4.10 4.11 4.17 4.19
68	PMIC_ON_REQ	5.3.1		67	MQS2_RIGHT UART5_TX CAN2_RX JTAG_TDO GPIO3_IO[31]	4.3.3 4.10 4.11 4.17 4.19
70	SAI1_TXC UART1_DSR UART2_CTS CAN1_RX SPI1_SIN GPIO1_IO[12]	4.3.2 4.10 4.10 4.11 4.12 4.19		69	V_SOM	5.1
72	UART3_TX UART4_TXD UART8_CTS SPI8_SOUT GPIO2_IO[14]	4.10 4.10 4.10 4.12 4.19		71	MQS2_LEFT UART5_RX CAN2_TX JTAG_TDI GPIO3_IO[28]	4.3.3 4.10 4.11 4.17 4.19

74	UART1_TXD/BT_MODE0 SPI2_PCS0 TPM1_CH1 GPIO1_IO[5]	4.10 4.12 4.15 4.19		73	UART5_CTS_B CAN4_RX JTAG_TCK GPIO3_IO[30]	4.10 4.11 4.17 4.19
76	UART1_RXD SPI2_SIN TPM1_CH0 GPIO1_IO[4]	4.10 4.12 4.15 4.19		75	SAI5_RX_DATA[0] SAI5_TX_DATA[1] SD3_CLK XSPI_CLK GPIO3_IO[20]	4.3.2 4.3.2 4.8 4.9 4.19
78	GND	5.1		77	SAI5_RXFS SAI5_TX_DATA[2] SD3_CMD XSPI_SS0_B GPIO3_IO[21]	4.3.2 4.3.2 4.8 4.9 4.19
80	LVDS0_CLK_P	4.1.2		79	SPDIF_IN SD3_CLK CAN5_TX I2C5_SDA TPM5_CH1 TPM6_EXTCLK GPIO2_IO[22]	4.3.1 4.8 4.11 4.13 4.15 4.15 4.19
82	LVDS0_CLK_N	4.1.2		81	SPDIF_OUT SD3_CMD CAN5_RX I2C5_SCL TPM6_CH1 GPIO2_IO[23]	4.3.1 4.8 4.11 4.13 4.15 4.19
84	SAI1_MCLK UART1_CTS UART2_RXD SPI2_SOUT TPM1_CH2 GPIO1_IO[6]	4.3.2 4.10 4.10 4.12 4.15 4.19		83	V_SOM	5.1
86	UART1_RTS UART2_TXD/BT_MODE1 SPI2_SCLK TPM1_CH3 GPIO1_IO[7]	4.10 4.10 4.12 4.15 4.19		85	PCIE2_CLK_REQ UART6_RTS SPI4_SIN GPIO5_IO[15]	4.5 4.10 4.12 4.19
88	GND	5.1		87	UART5_RTS_B SPI6_SCLK I2C4_SCL I2C6_SCL GPIO2_IO[3]	4.10 4.12 4.13 4.13 4.19
90	ALT_BOOT#	5.5		89	UART5_CTS_B SPI6_SOUT I2C4_SDA I2C6_SDA GPIO2_IO[2]	4.10 4.12 4.13 4.13 4.19
92	SAI1_TXD/BT_MODE3 UART1_DTR UART2_RTS CAN1_TX SPI1_SCLK GPIO1_IO[13]	4.3.2 4.10 4.10 4.11 4.12 4.19		91	CAN3_TX I2C3_SDA GPIO2_IO[28]	4.11 4.13 4.19
94	CAN3_RX I2C3_SCL GPIO2_IO[29]	4.11 4.13 4.19		93	VCC_RTC	5.1
96	UART7_CTS SPI3_SOUT I2C8_SDA TPM4_EXTCLK GPIO2_IO[10]	4.10 4.12 4.13 4.15 4.19		95	SAI1_TX_DATA[1] SAI1_TXFS/BT_MODE2 MQS1_LEFT UART2_DTR SPI1_PCS0 GPIO1_IO[11]	4.3.2 4.3.2 4.3.3 4.10 4.12 4.19
98	SAI1_MCLK SAI1_RX_DATA[0] MQS1_RIGHT UART2_DSR SPI1_SOUT GPIO1_IO[14]	4.3.2 4.3.2 4.3.3 4.10 4.12 4.19		97	UART7_TXD SPI3_PCS0 I2C7_SDA TPM6_CH0 GPIO2_IO[8]	4.10 4.12 4.13 4.15 4.19

100	UART7_RTS SPI3_SCLK I2C8_SCL TPM5_EXTCLK GPIO2_IO[11]	4.10 4.12 4.13 4.15 4.19		99	UART7_RXD SPI3_SIN I2C7_SCL TPM3_EXTCLK GPIO2_IO[9]	4.10 4.12 4.13 4.15 4.19

Table 72 Connector P2

Pin #	UCM-iMX95 Signal Name	Ref.		Pin #	UCM-iMX95 Signal Name	Ref.
2	MIPI_CSI_CLK_N	4.2		1	MIPI_DSICSI_D0_N	4.1.1 4.2
4	MIPI_CSI_CLK_P	4.1.2		3	MIPI_DSICSI_D0_P	4.1.1 4.2
6	MIPI_CSI_D0_N	4.1.2		5	MIPI_DSICSI_D2_N	4.1.1 4.2
8	MIPI_CSI_D0_P	4.1.2		7	MIPI_DSICSI_D2_P	4.1.1 4.2
10	GND	5.1		9	V_SOM	5.1
12	LVDS1_D0_P	4.1.2		11	MIPI_DSICSI_D3_N	4.1.1 4.2
14	LVDS1_D0_N	4.1.2		13	MIPI_DSICSI_D3_P	4.1.1 4.2
16	GND	5.1		15	MIPI_DSICSI_D1_N	4.1.1 4.2
18	LVDS1_D1_P	4.1.2		17	MIPI_DSICSI_D1_P	4.1.1 4.2
20	LVDS1_D1_N	4.1.2		19	V_SOM	5.1
22	GND	5.1		21	MIPI_DSICSI_CLK_N	4.1.1 4.2
24	LVDS1_D2_P	4.1.2		23	MIPI_DSICSI_CLK_P	4.1.1 4.2
26	LVDS1_D2_N	4.1.2		25	MIPI_CSI_D2_N	4.2
28	GND	5.1		27	MIPI_CSI_D2_P	4.2
30	PCIE1_RX0_N	4.5		29	V_SOM	5.1
32	PCIE1_RX0_P	4.2		31	MIPI_CSI_D1_N	4.2
34	GND	5.1		33	MIPI_CSI_D1_P	4.2
36	PCIE1_TX0_N	4.5		35	MIPI_CSI_D3_N	4.2
38	PCIE1_TX0_P	4.5		37	MIPI_CSI_D3_P	4.2
40	GND	5.1		39	V_SOM	5.1
42	PCIE1_CLKIN_P	4.5		41	SAI2_TX_DATA[2] SAI4_RX_BCLK ENET2_RD0 UART4_RXD GPIO4_IO[24]	4.3.2 4.3.2 4.4.3 4.10 4.19
44	PCIE1_CLKIN_N	4.5		43	SPDIF_IN SAI2_TX_DATA[3] SAI4_RX_DATA[0] ENET2_RD1 GPIO4_IO[25]	4.3.1 4.3.2 4.3.2 4.4.3 4.19
46	GND	5.1		45	SAI2_MCLK MQS2_RIGHT ENET2_RD2 UART4_CTS GPIO4_IO[26]	4.3.2 4.3.3 4.4.3 4.10 4.19
48	LVDS1_D3_P	4.1.2		47	SPDIF_IN SPDIF_OUT MQS2_LEFT ENET2_RD3 GPIO4_IO[27]	4.3.1 4.3.1 4.3.3 4.4.3 4.19
50	LVDS1_D3_N	4.1.2		49	CAN3_TX CCM_CLKO3 GPIO4_IO[28]	4.11 4.18 4.19

52	CAN3_RX CCM_CLKO4 GPIO4_IO[29]	4.11 4.18 4.19		51	SD2_RESET# GPIO3_IO[7]	4.8 4.19
54	GND	5.1		53	SAI2_TX_DATA[0] ENET2_RX_CTL UART4_DSR GPIO4_IO[22]	4.3.2 4.4.3 4.10 4.19
56	LVDS1_CLK_P	4.1.2		55	SAI2_TX_DATA[1] SAI4_RXFS ENET2_RXC GPIO4_IO[23]	4.3.2 4.3.2 4.4.3 4.19
58	LVDS1_CLK_N	4.1.2		57	V_SOM	5.1
60	SAI2_RX_BCLK ENET2_MDIO UART4_RIN GPIO4_IO[15]	4.3.2 4.4.3 4.10 4.19		59	SAI2_RX_DATA[3] SAI4_TX_DATA[0] ENET2_TD0 UART4_TXD GPIO4_IO[19]	4.3.2 4.3.2 4.4.3 4.10 4.19
62	SD2_VSEL GPIO3_IO[19]	5.3.2 4.19		61	SAI2_RX_DATA[2] SAI4_TX_BCLK ENET2_TD1 UART4_RTS GPIO4_IO[18]	4.3.2 4.3.2 4.4.3 4.10 4.19
64	ONOFF	5.3.1		63	SAI2_RX_DATA[1] SAI4_TXFS ENET2_TD2 GPIO4_IO[17]	4.3.2 4.3.2 4.4.3 4.19
66	POR_B_3V3	5.3.2 5.4		65	SAI2_RX_DATA[0] ENET2_TD3 GPIO4_IO[16]	4.3.2 4.4.3 4.19
68	ENET1_MDC GPIO4_IO[0]	4.4.3 4.19		67	SAI2_TXFS ENET2_TX_CTL UART4_DTR GPIO4_IO[20]	4.3.2 4.4.3 4.10 4.19
70	ENET1_MDIO GPIO4_IO[1]	4.4.3 4.19		69	SAI2_TX_BCLK ENET2_TXC GPIO4_IO[21]	4.3.2 4.4.3 4.19
72	GND	5.1		71	V_SOM	5.1
74	ETH1_MDI0P	4.4.2		73	ETH1_MDI0N	4.4.2
76	SAI2_RXFS ENET2_MDC UART4_DCB GPIO4_IO[14]	4.3.2 4.4.3 4.10 4.19		75	ETH1_LED2/CFG_LDO1	4.4.2
78	ETH1_MDI1P	4.4.2		77	RESERVED	5.9
80	ETH1_MDI1N	4.4.2		79	ETH1_MDI2P	4.4.2
82	GND	5.1		81	ETH1_MDI2N	4.4.2
84	ETH1_MDI3P	4.4.2		83	ETH1_LED1/CFG_LDO0	4.4.2
86	ETH1_LED0/CFG_EXT	4.4.2		85	ETH1_MDI3N	4.4.2
88	SDP_BOOT#	5.5		87	V_SOM	5.1
90	PCIE1_CLK_REQ UART6_TXD SPI4_PCS2 GPIO5_IO[12]	4.5 4.10 4.12 4.19		89	PDM_BIT_STREAM0 UART6_RXD CAN4_RX SPI7_SIN I2C6_SCL TPM4_CH0 GPIO2_IO[5]	4.3.4 4.10 4.11 4.12 4.13 4.15 4.19
92	SD2_CD# I3C2_SCL GPIO3_IO[0]	4.8 4.14 4.19		91	PDM_CLK UART6_TXD CAN4_TX SPI7_PCS0 I2C6_SDA TPM3_CH0 GPIO2_IO[4]	4.3.4 4.10 4.11 4.12 4.13 4.15 4.19

94	MQS2_RIGHT SD2_DATA2 GPIO3_IO[5]	4.3.3 4.8 4.19		93	UART6_RTS SPI3_PCS1 SPI7_SCLK I2C7_SCL GPIO2_IO[7]	4.10 4.12 4.12 4.13 4.19
96	SD2_CLK I3C2_SDA GPIO3_IO[1]	4.8 4.14 4.19		95	PDM_BIT_STREAM1 UART6_CTS SPI7_SOUT I2C7_SDA TPM5_CH0 GPIO2_IO[6]	4.3.4 4.10 4.12 4.13 4.15 4.19
98	MQS2_LEFT SD2_DATA3 GPIO3_IO[6]	4.3.3 4.8 4.19		97	SD2_DATA0 CAN2_TX GPIO3_IO[3]	4.8 4.11 4.19
100	SD2_CMD I3C2_PUR GPIO3_IO[2]	4.8 4.14 4.19		99	SD2_DATA1 CAN2_RX GPIO3_IO[4]	4.8 4.11 4.19

Table 73 Connector P3

Pin #	UCM-iMX95 Signal Name	Ref.		Pin #	UCM-iMX95 Signal Name	Ref.
2	MQS1_LEFT PDM_CLK CAN1_TX GPIO1_IO[8]	4.3.3 4.3.4 4.11 4.19		1	ADC_IN0	4.16
4	MQS1_RIGHT PDM_BIT_STREAM0 CAN1_RX SPI1_PCS1 TPM1_EXTCLK GPIO1_IO[9]	4.3.3 4.3.4 4.11 4.12 4.15 4.19		3	ADC_IN1	4.16
6	PDM_BIT_STREAM1 SPI2_PCS1 GPIO1_IO[10]	4.3.4 4.12 4.19		5	ADC_IN2	4.16
8	GND	5.1		7	ADC_IN3	4.16
10	SAI2_TX_DATA[4] SAI4_RXFS XSPI_CLK GPIO5_IO[9]	4.3.2 4.3.2 4.9 4.19		9	GND	5.1
12	GND	5.1		11	ADC_IN4	4.16
14	SAI2_TX_DATA[6] SAI5_RXFS SAI5_TX_DATA[2] XSPI_DQS GPIO5_IO[8]	4.3.2 4.3.2 4.3.2 4.9 4.19		13	ADC_IN5	4.16
16	SAI2_TX_DATA[7] SAI5_RX_BCLK SAI5_TX_DATA[3] XSPI_SS1_B GPIO5_IO[11]	4.3.2 4.3.2 4.3.2 4.9 4.19		15	ADC_IN6	4.16
18	GND	5.1		17	ADC_IN7	4.16
20	SAI2_TX_DATA[5] SAI4_RX_BCLK XSPI_SS0_B GPIO5_IO[10]	4.3.2 4.3.2 4.9 4.19		19	GND	5.1
22	SAI2_TX_DATA[4] SAI4_RX_DATA[1] SAI4_TX_BCLK XSPI_DATA0 GPIO5_IO[0]	4.3.2 4.3.2 4.3.2 4.9 4.19		21	CCM_CLKO2 GPIO3_IO[27]	4.18 4.19
24	SAI2_TX_DATA[5] SAI4_TX_DATA[1] SAI4_TXFS XSPI_DATA1 GPIO5_IO[1]	4.3.2 4.3.2 4.3.2 4.9 4.19		23	GND	5.1
26	GND	5.1		25	ETH_CLKIN_P	4.4.1

28	SAI2_TX_DATA[6] SAI4_TX_DATA[0] XSPI_DATA2 GPIO5_IO[2]	4.3.2 4.3.2 4.9 4.19		27	ETH_CLKIN_N	4.4.1
30	SAI2_TX_DATA[7] SAI4_RX_DATA[0] XSPI_DATA3 GPIO5_IO[3]	4.3.2 4.3.2 4.9 4.19		29	GND	5.1
32	SAI5_RX_DATA[1] SAI5_TX_DATA[0] XSPI_DATA4 GPIO5_IO[4]	4.3.2 4.3.2 4.9 4.19		31	ETH_TX0_P	4.4.1
34	GND	5.1		33	ETH_TX0_N	4.4.1
36	SAI2_TX_DATA[6] SAI5_RX_DATA[2] SAI5_TXFS XSPI_DATA5 GPIO5_IO[5]	4.3.2 4.3.2 4.3.2 4.9 4.19		35	GND	5.1
38	SAI2_TX_DATA[7] SAI5_RX_DATA[3] SAI5_TX_BCLK XSPI_DATA6 GPIO5_IO[6]	4.3.2 4.3.2 4.3.2 4.9 4.19		37	ETH_RX0_P	4.4.1
40	SAI5_RX_DATA[0] SAI5_TX_DATA[1] XSPI_DATA7 GPIO5_IO[7]	4.3.2 4.3.2 4.9 4.19		39	ETH_RX0_N	4.4.1

6.2 Mating Connectors

Table 74 Connector type

UCM-iMX95 connector		Carrier board (mating) connector P/N		
Ref.	Implementation	Mfg.	P/N	Mating Height
P1, P2	Hirose DF40C-100DP-0.4V51	Hirose	DF40HC(3.0)-100DS-0.4V(51)	3.0mm
P3	Hirose DF40C-40DP-0.4V51	Hirose	DF40HC(3.0)-40DS-0.4V(51)	3.0mm

6.3 Mechanical Drawings

- All dimensions are in millimeters.
- The height of top side components is < 1.8mm.
- Carrier-board connectors provide 3.0 ± 0.15mm board-to-board clearance.
- Board thickness is 1.6mm.

3D model and mechanical drawings in DXF format are available at https://www.compulab.com/products/computer-on-modules/ucm-imx95-nxp-i-mx-95-som-system-on-module/#devres

Figure 3 UCM-iMX95 top

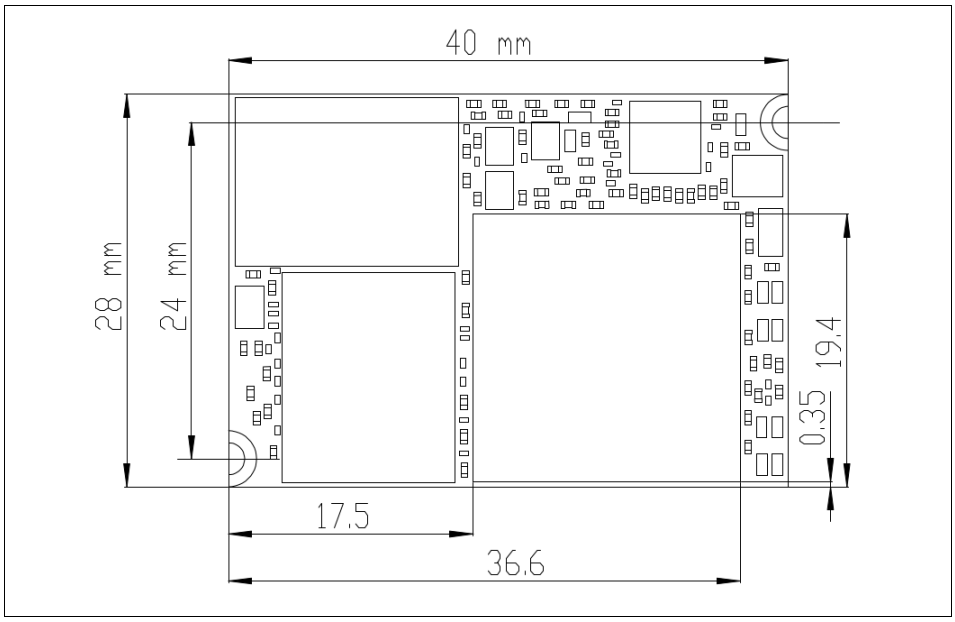
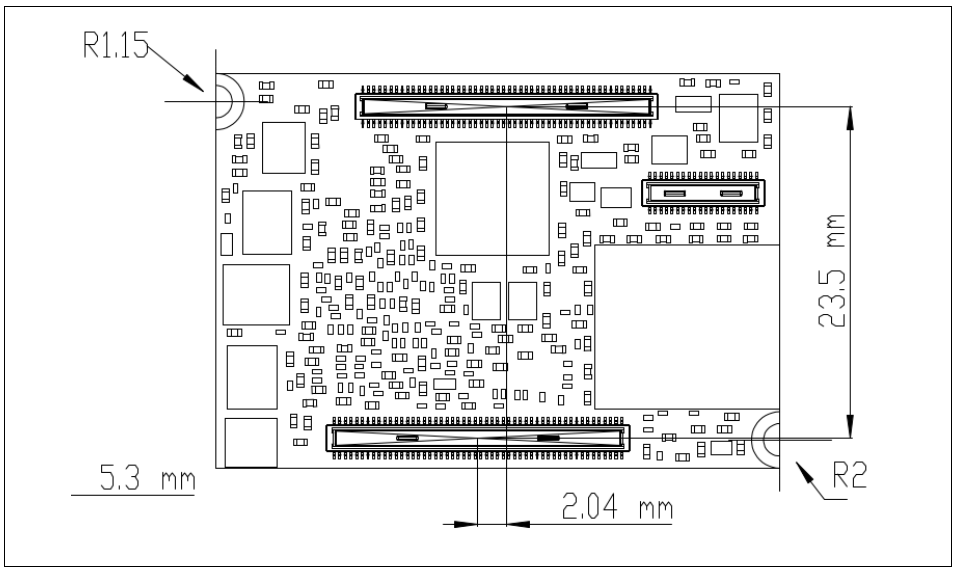


Figure 4 UCM-iMX95 bottom



6.4 Heat Spreader and Cooling Solutions

Compulab provides UCM-iMX95 with an optional heat-spreader assembly. The UCM-iMX95 heat-spreader has been designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the UCM-iMX95 temperature specifications. Various thermal management solutions can be used with the heat-spreader, including active and passive approaches.

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 75 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	6.0	V
Voltage on any non-power supply pin	-0.5	3.6	V
Backup battery supply voltage (VCC_RTC)	-0.3	3.8	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 76 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.45	3.7	5.5	V
Backup battery supply voltage (VCC_RTC)	1.5	3.0	3.6	V

7.3 ESD Performance

Table 77 ESD Performance

Interface	ESD Performance
i.MX95 pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V_SOM and GND near the mating connectors.
- Except for a power connection, no other connection is mandatory for UCM-iMX95 operation. All power-up circuitry and all required pullups/pulldowns are available onboard UCM-iMX95.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- Bear in mind that there are components on the bottom side of UCM-iMX95. It is not recommended to place any components underneath the UCM-iMX95 module.
- Refer to the SB-UCMIMX95 carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise, corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.

- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from UCM-iMX95, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-UCMIMX95 carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.